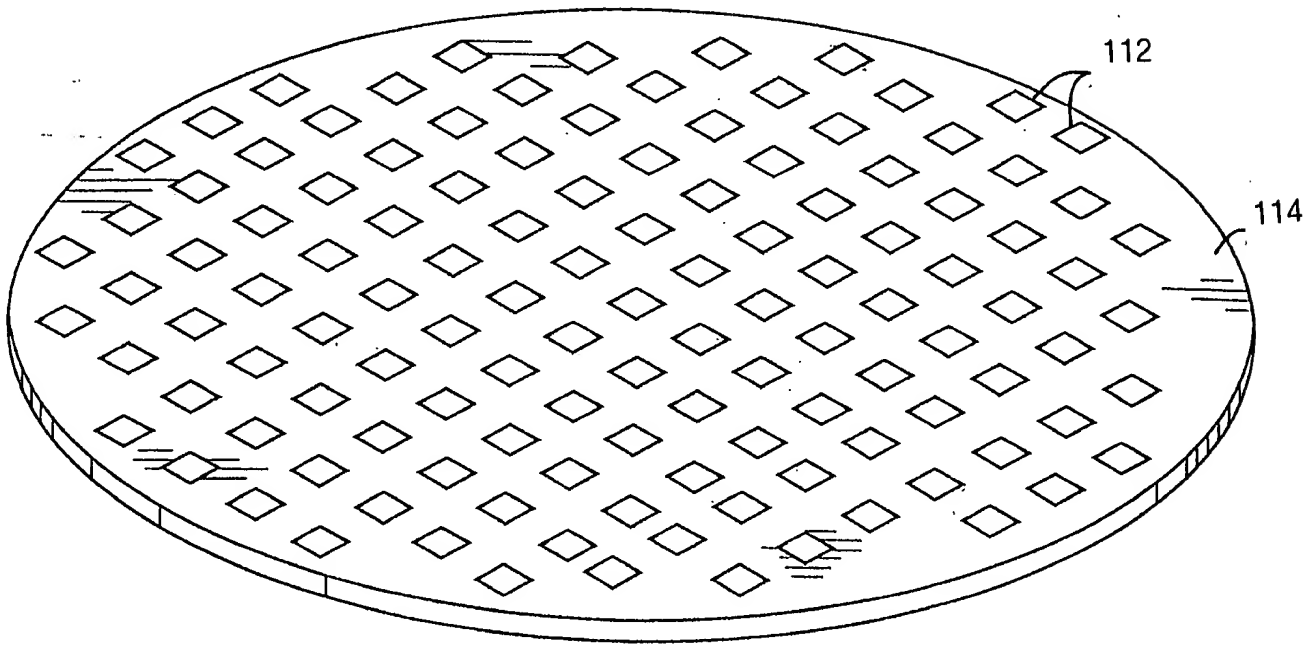


FIG. 1

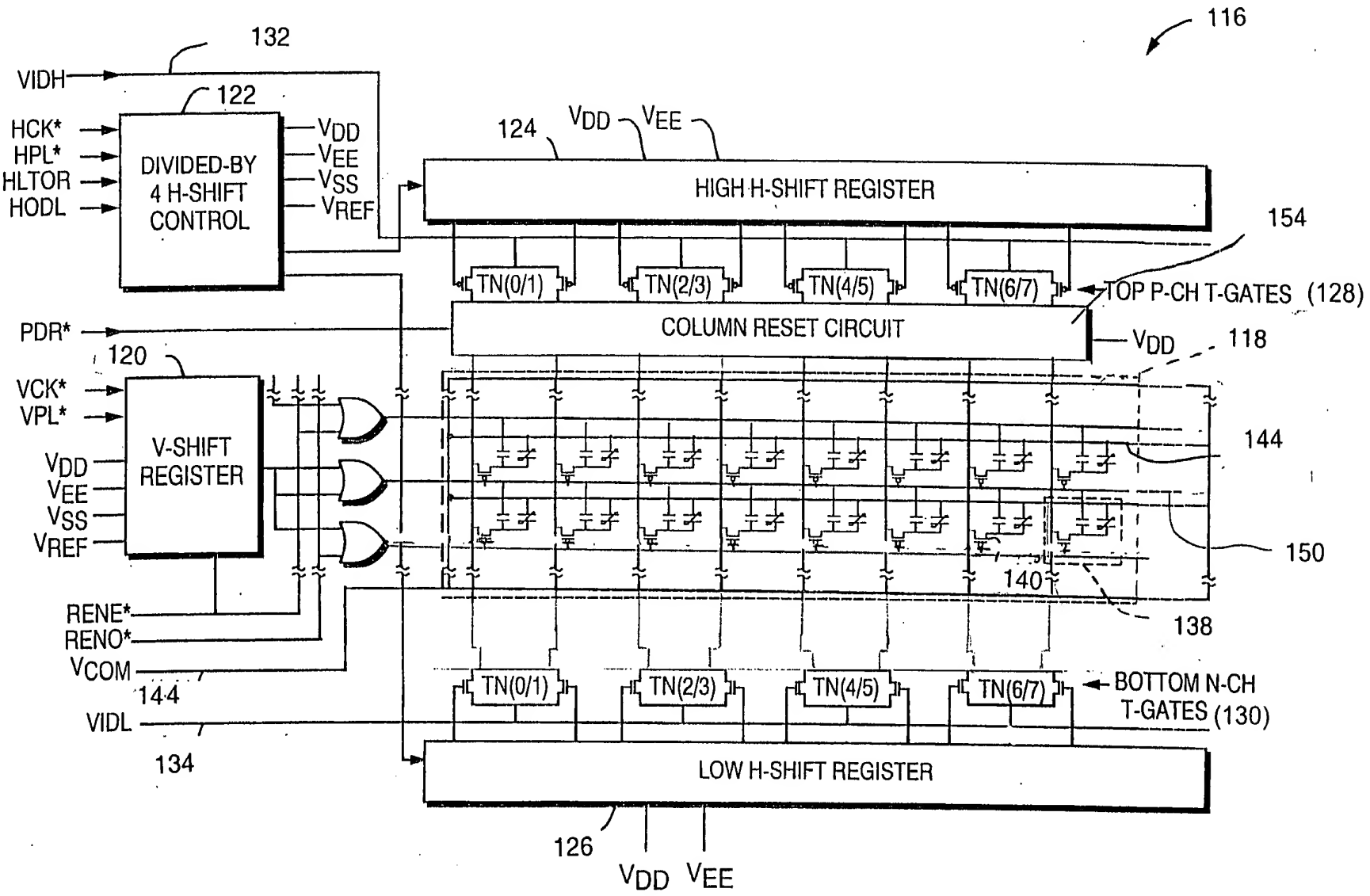
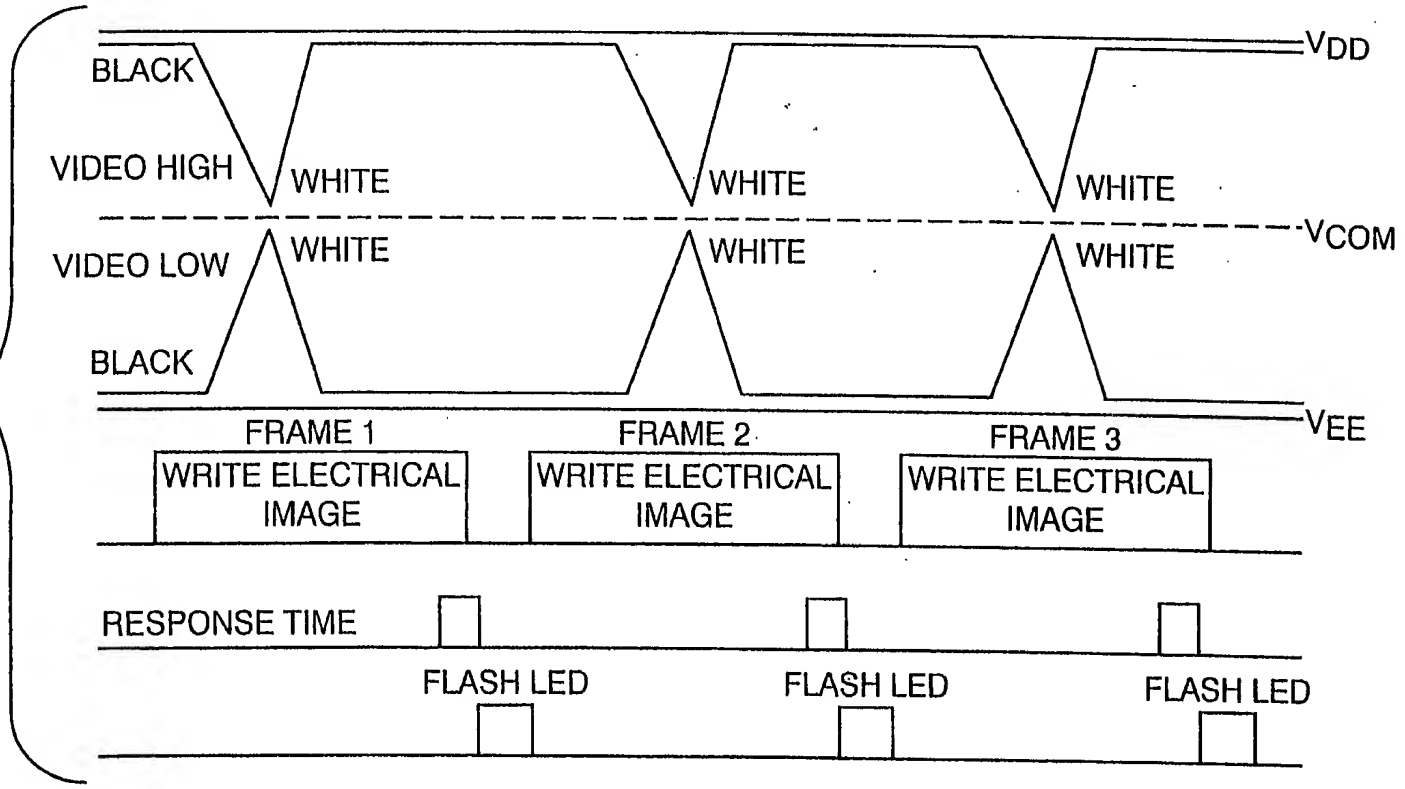


FIG. 2

FIG. 3



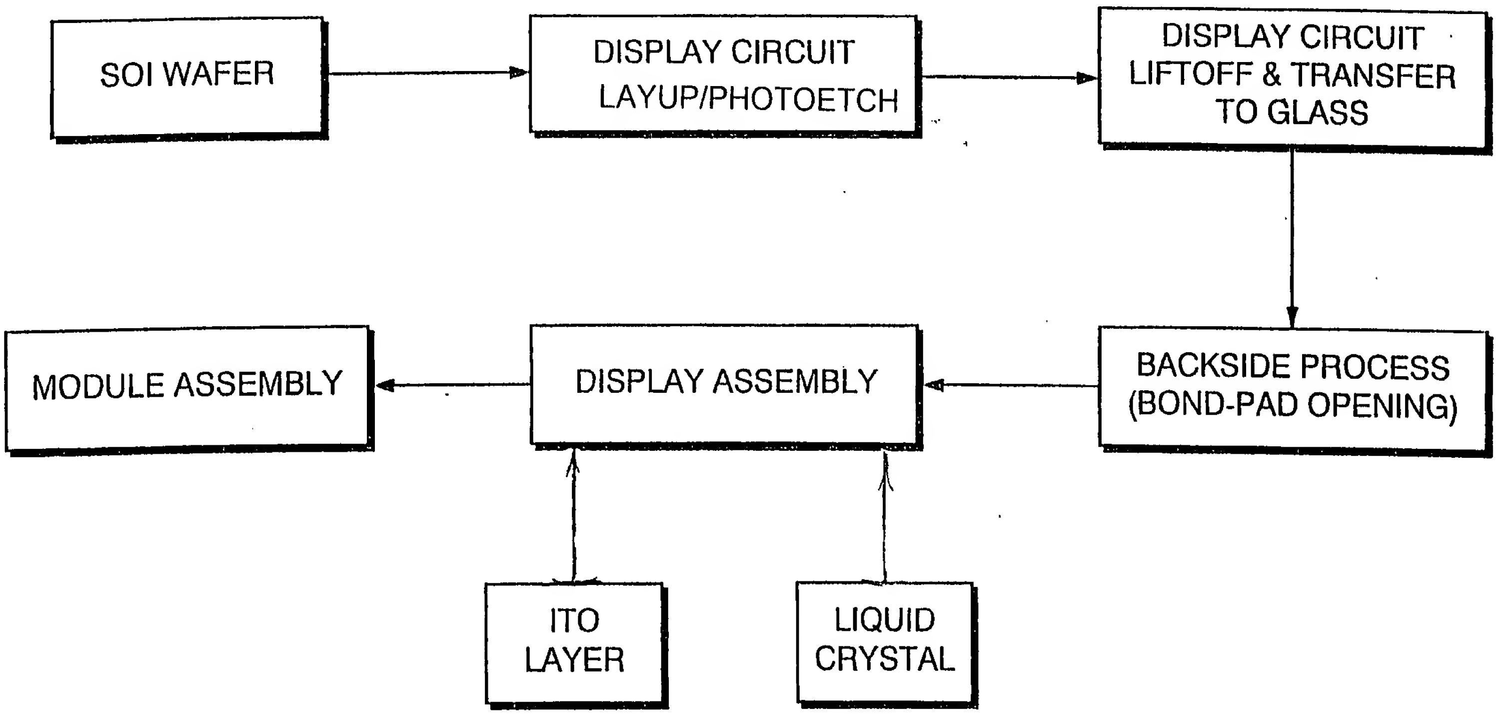

SOI WAFER
DISPLAY CIRCUIT LAYUP/PHOTOETCH
DISPLAY CIRCUIT LIFTOFF & TRANSFER TO GLASS
BACKSIDE PROCESS (BOND-PAD OPENING)
DISPLAY ASSEMBLY
MODULE ASSEMBLY
ITO LAYER
LIQUID CRYSTAL

FIG. 4

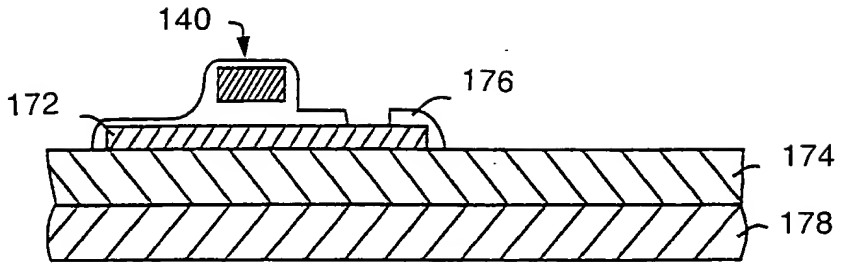


FIG. 5A

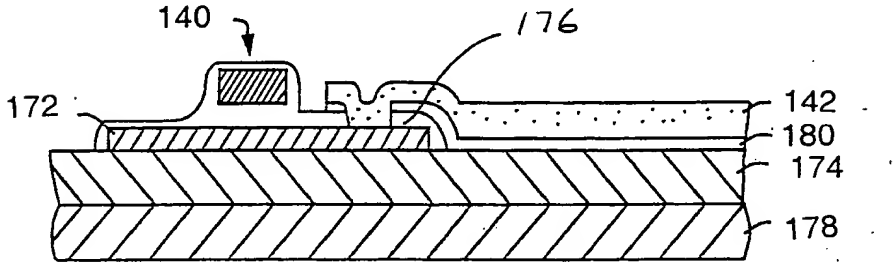


FIG. 5B

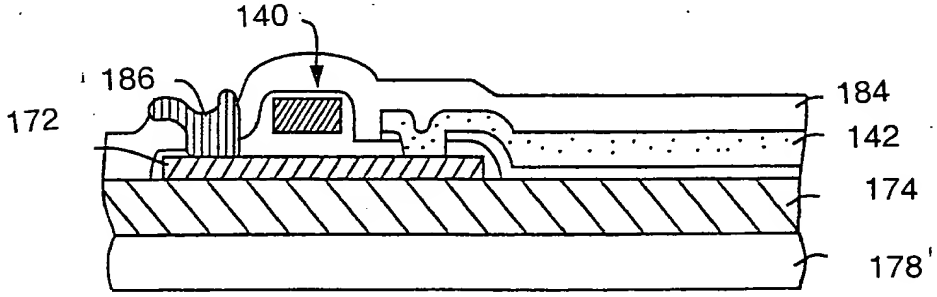


FIG. 5C

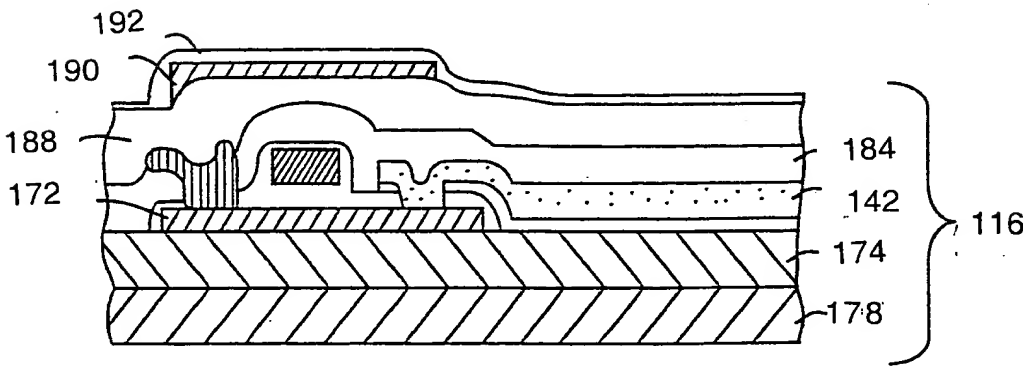


FIG. 5D

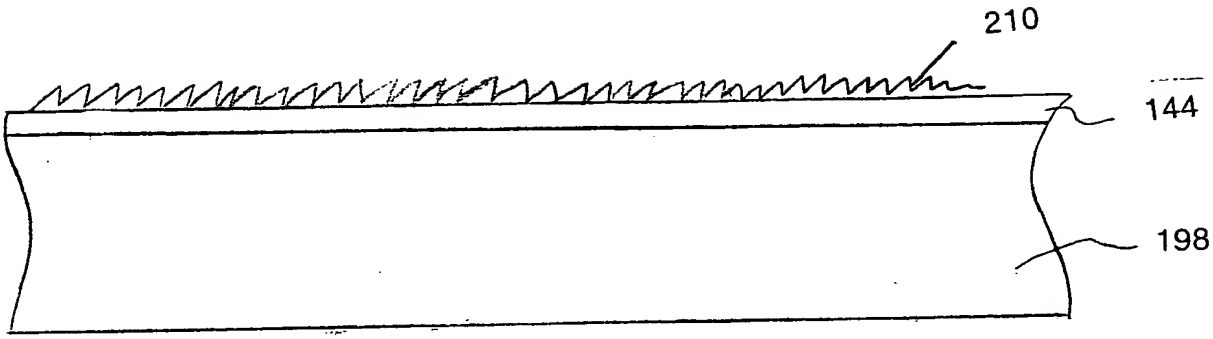


FIG. 6

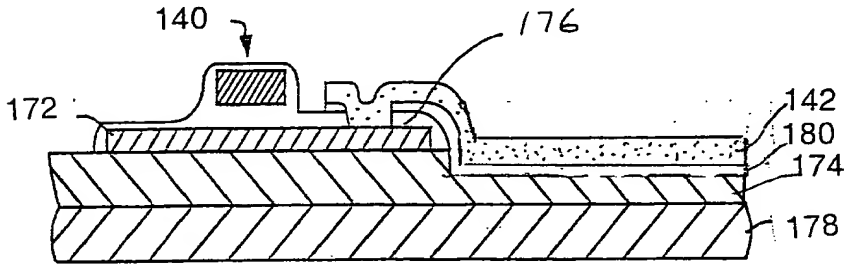


FIG. 7B

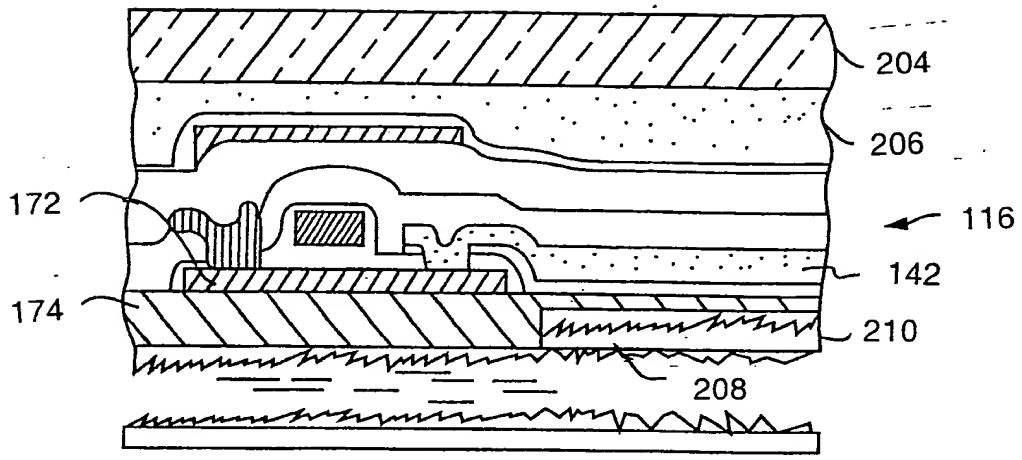


FIG. 7A

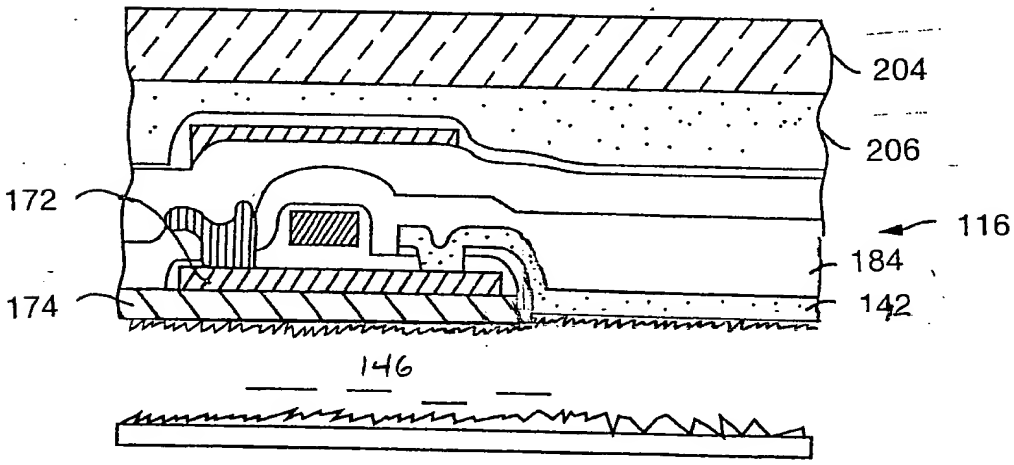
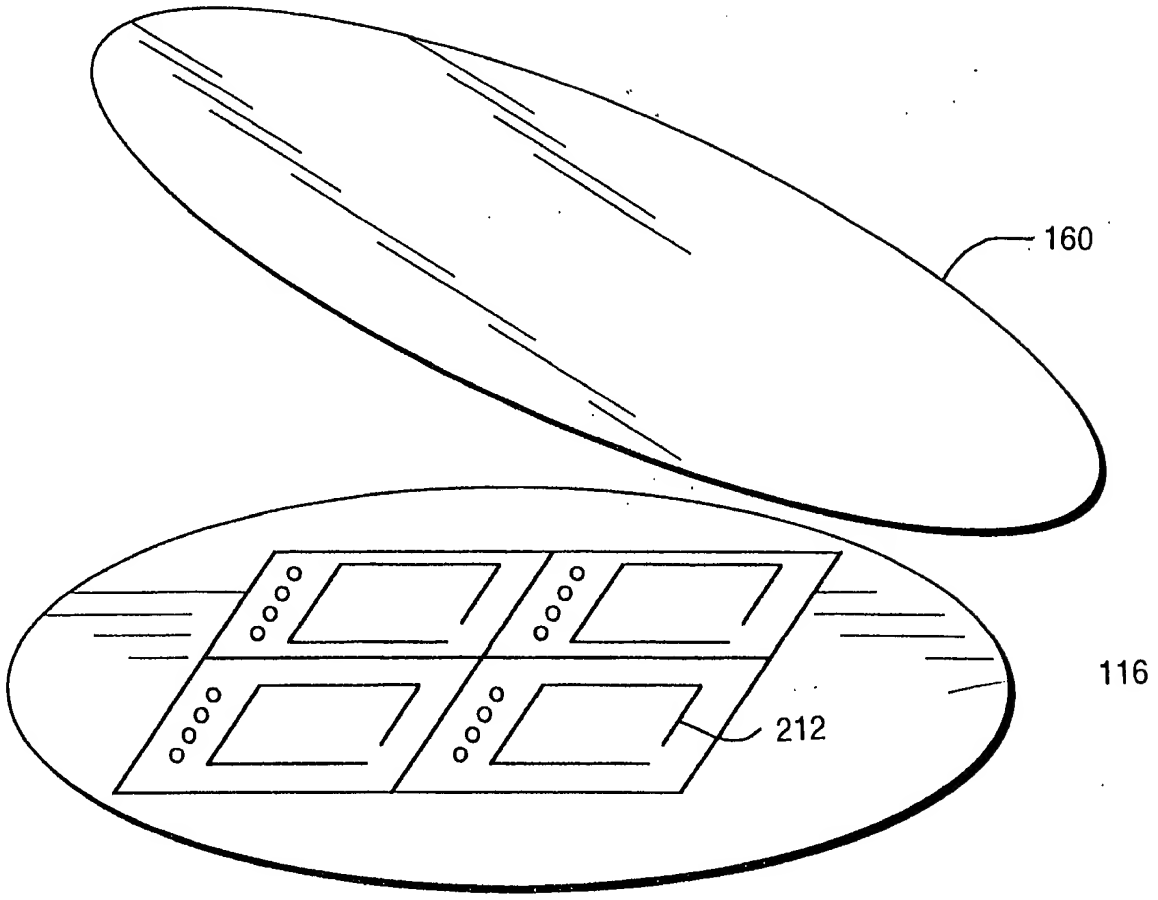


FIG. 7C

FIG. 8



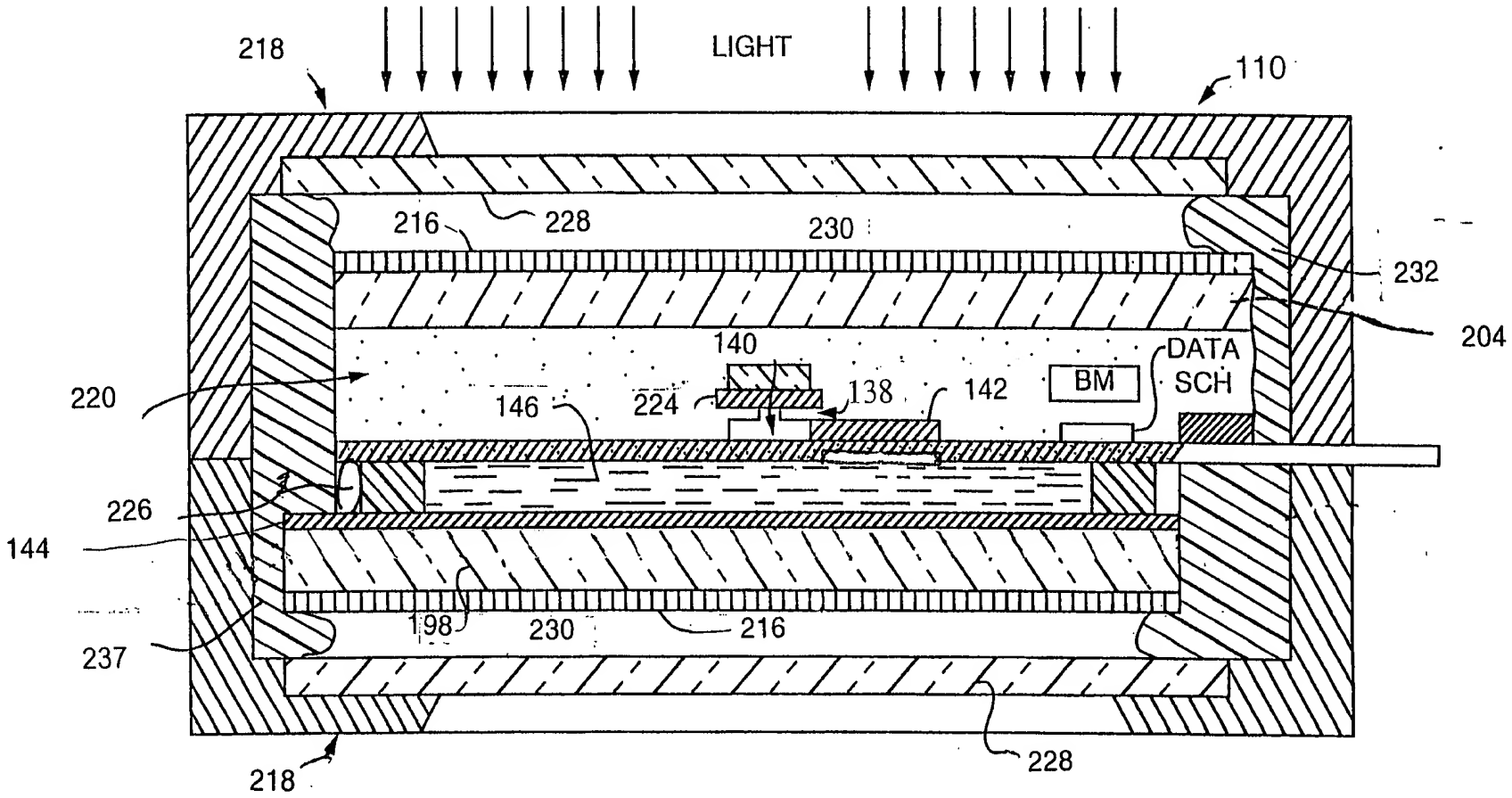

218
LIGHT
110
216
228
230
232
204
140
DATA
SCH
220
146
224
138
142
BM
226
144
198
230
216
237
218
228

FIG. 9

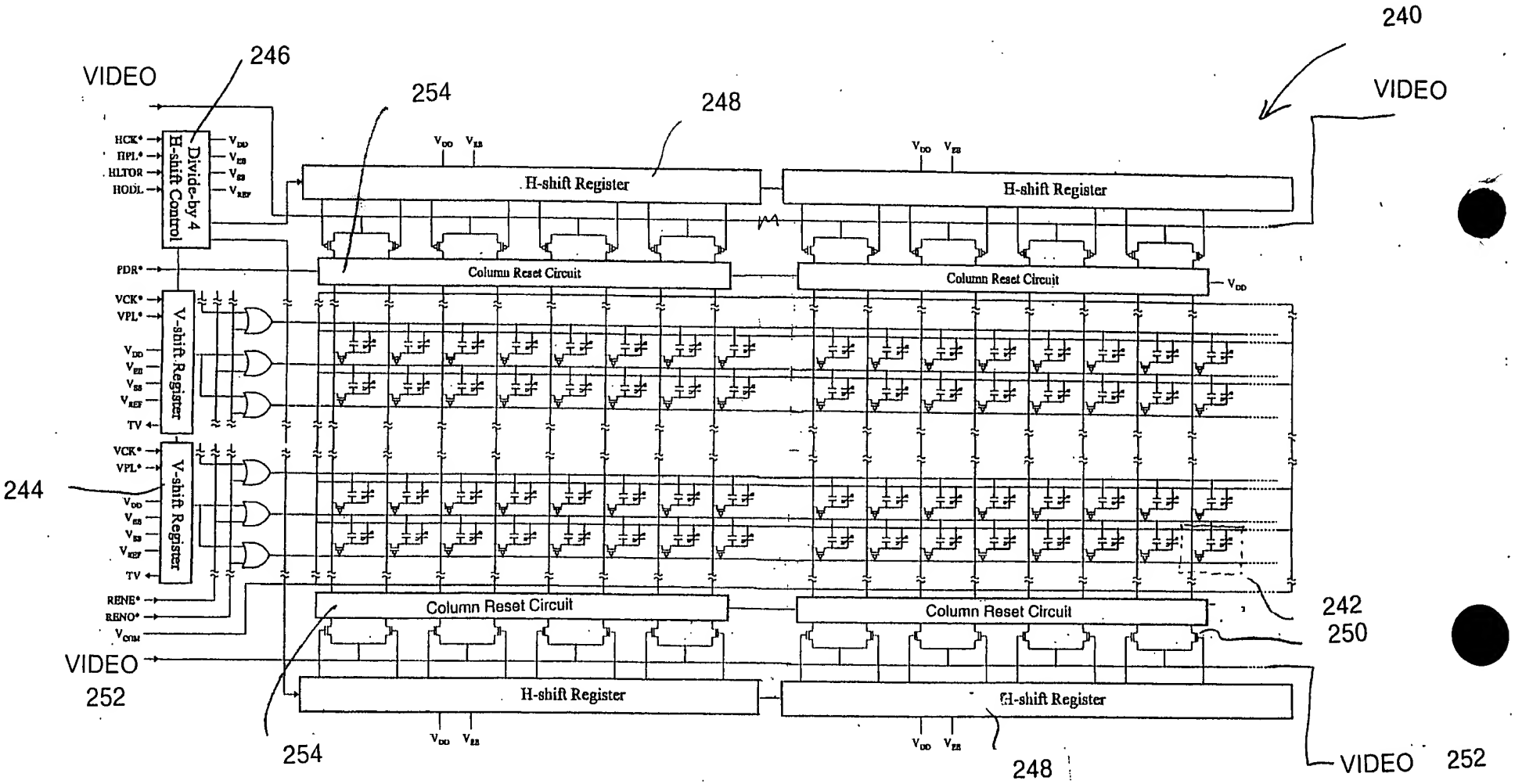
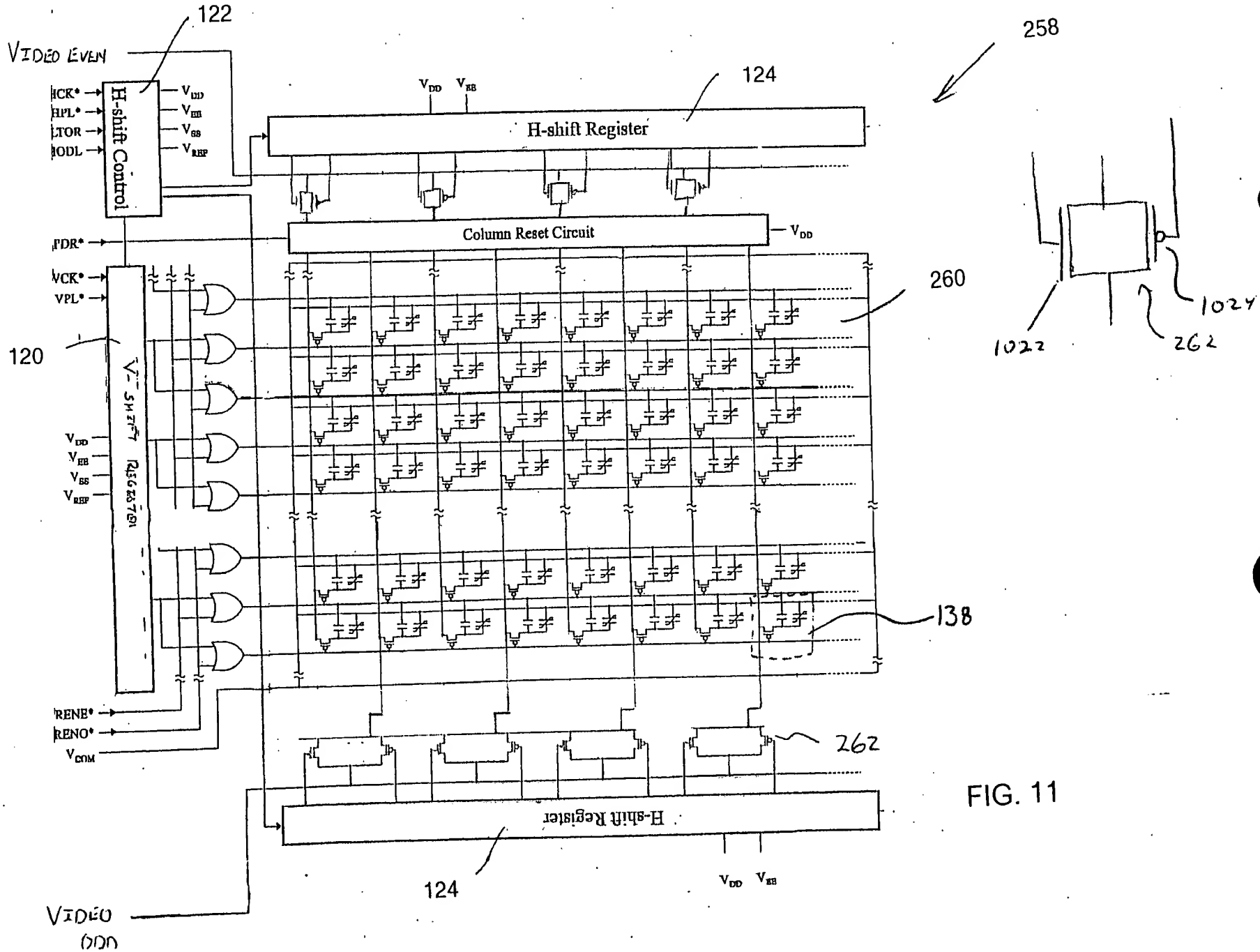

240
VIDEO
246
254
248
VIDEO
H-shift Register
H-shift Register
Column Reset Circuit
Column Reset Circuit
Column Reset Circuit
Column Reset Circuit
H-shift Register
H-shift Register
Divide-by 4
H-shift Control
V-shift Register
V-shift Register
244
242
250
VIDEO
252
254
248
VIDEO
252

FIG. 10


122
VIDEO EVEN
H-shift Control
V_{DD}
V_{EE}
V_{SS}
V_{REF}
124
H-shift Register
Column Reset Circuit
V_{DD}
260
120
V- shift Register
138
262
H-shift Register
124
VIDEO
ODD

258
1024
1022
262

FIG. 11

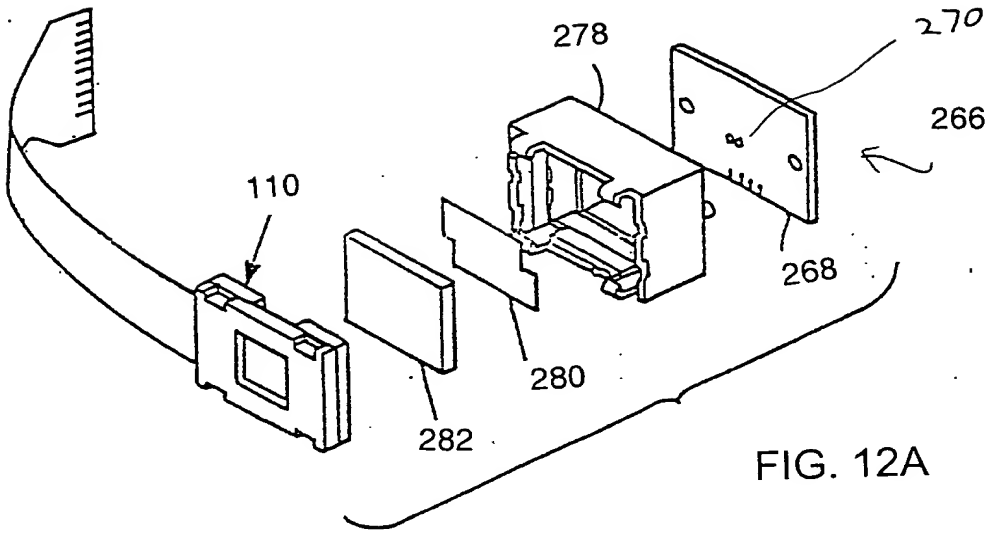


FIG. 12A

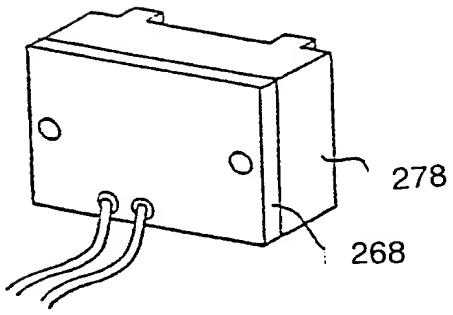


FIG. 12B

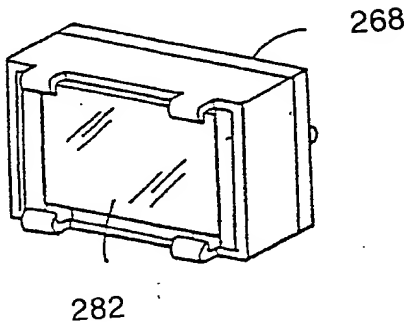


FIG. 12C

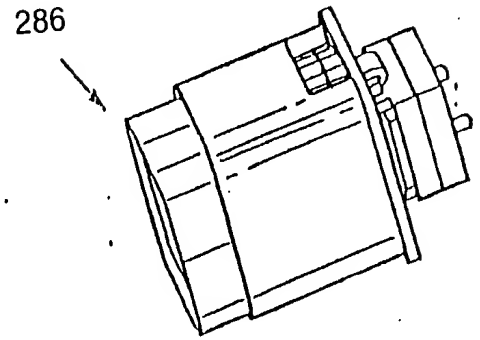


FIG. 13A

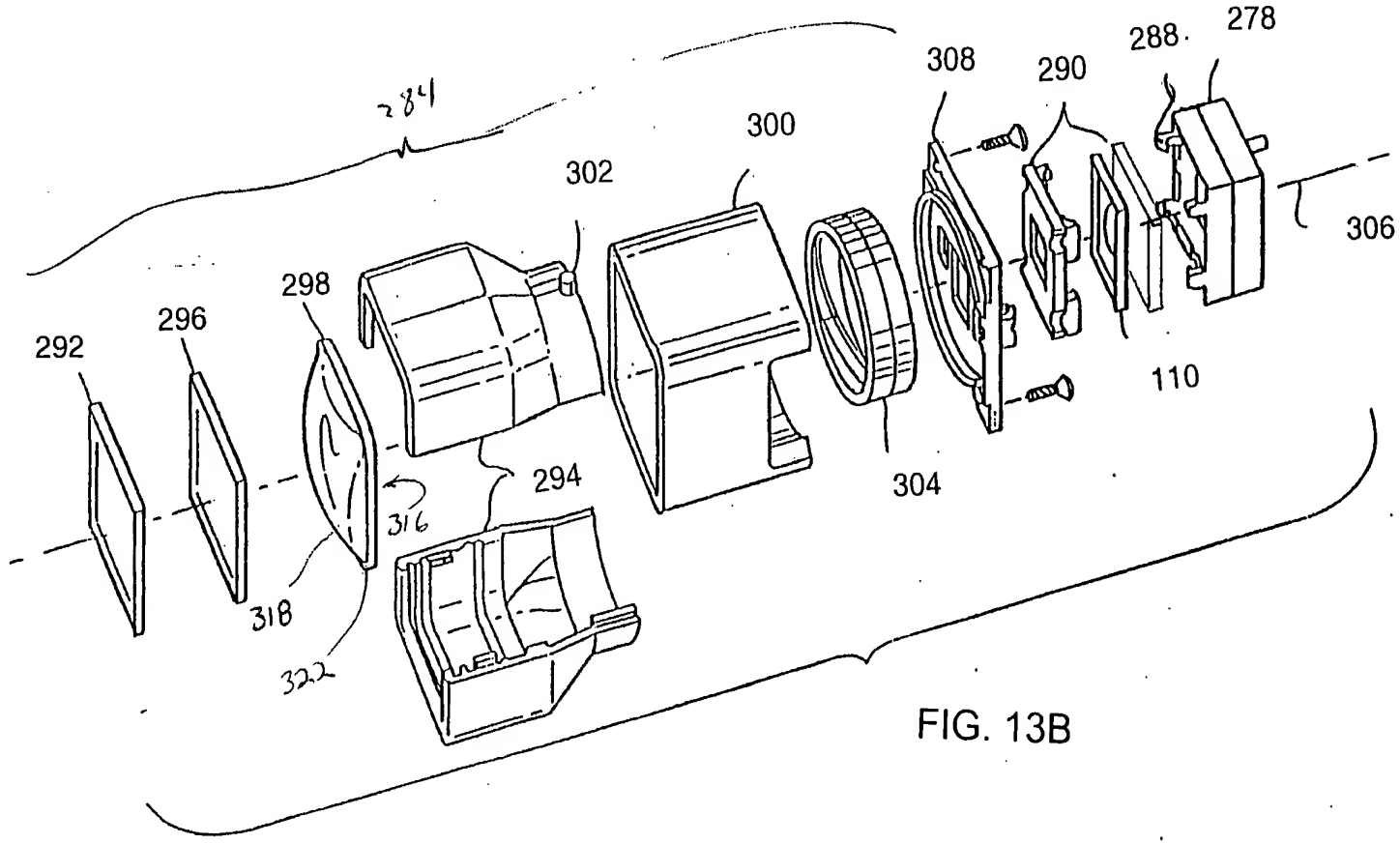


FIG. 13B

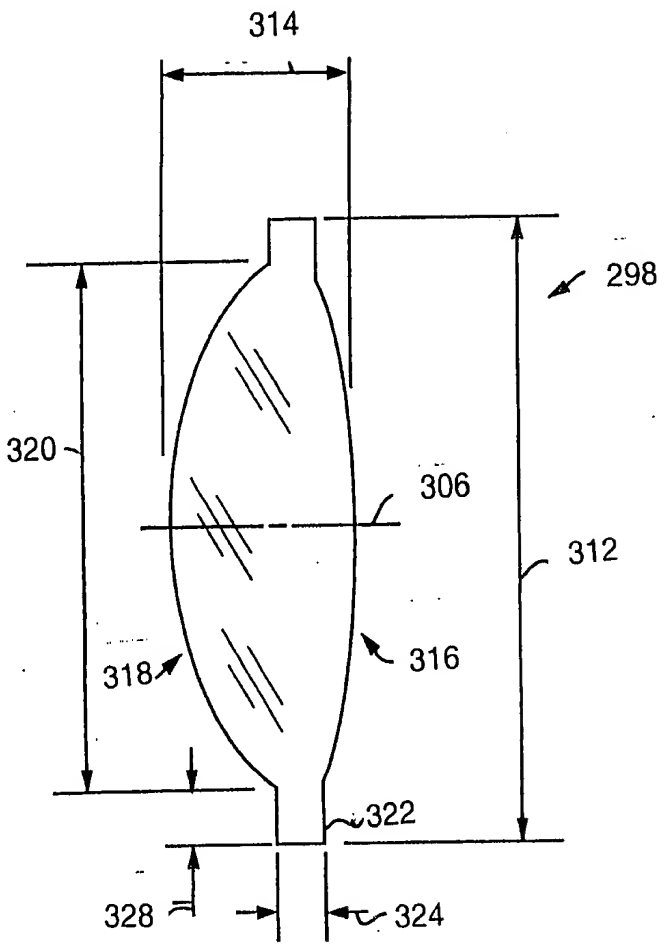


FIG. 14A

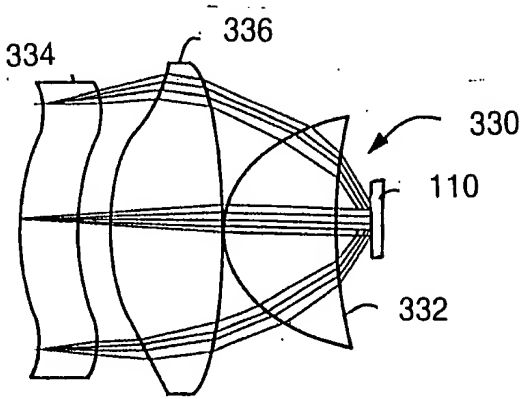


FIG. 14C

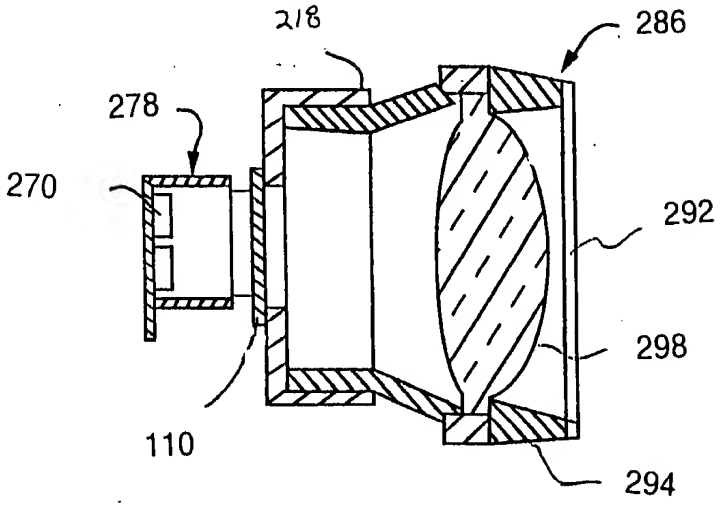


FIG. 14B

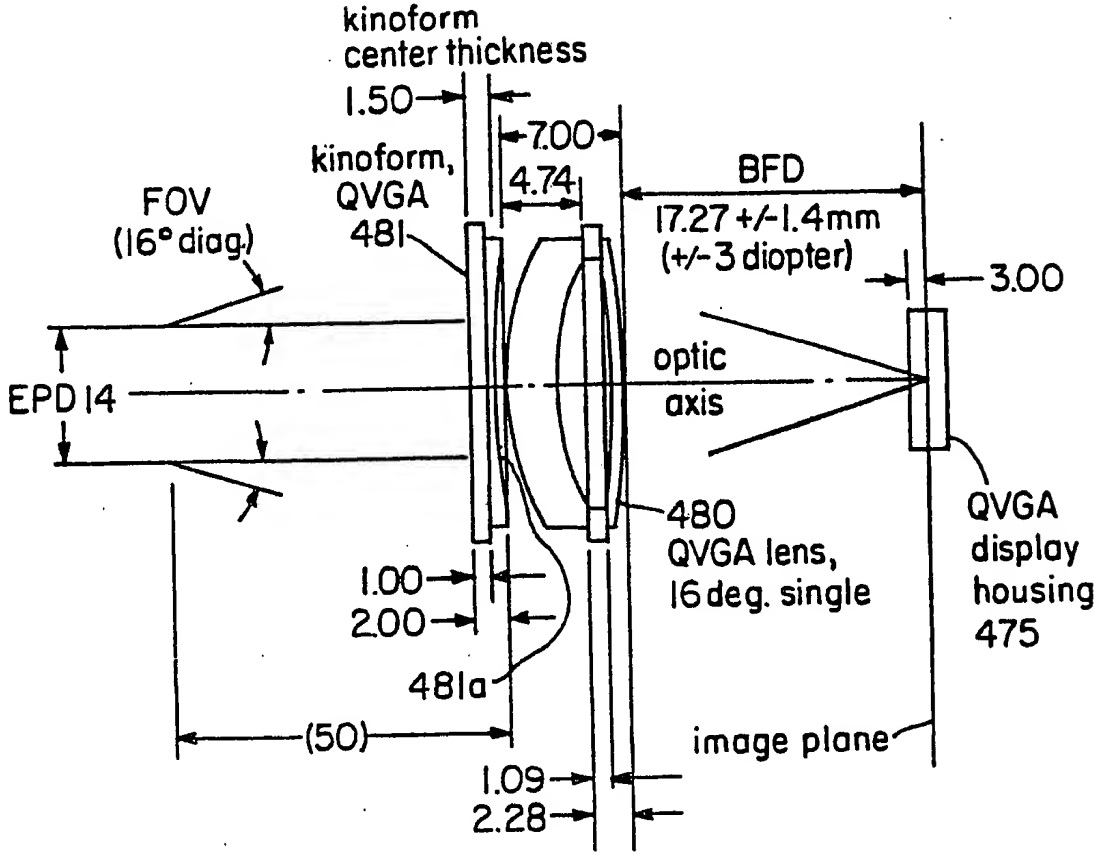


FIG. 15

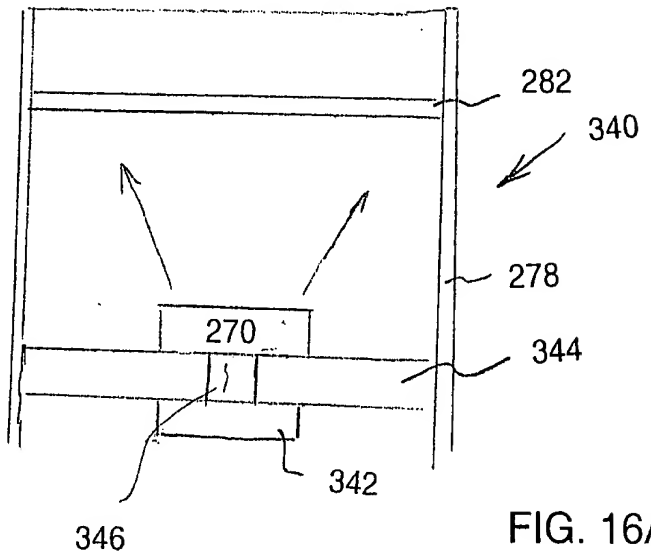


FIG. 16A

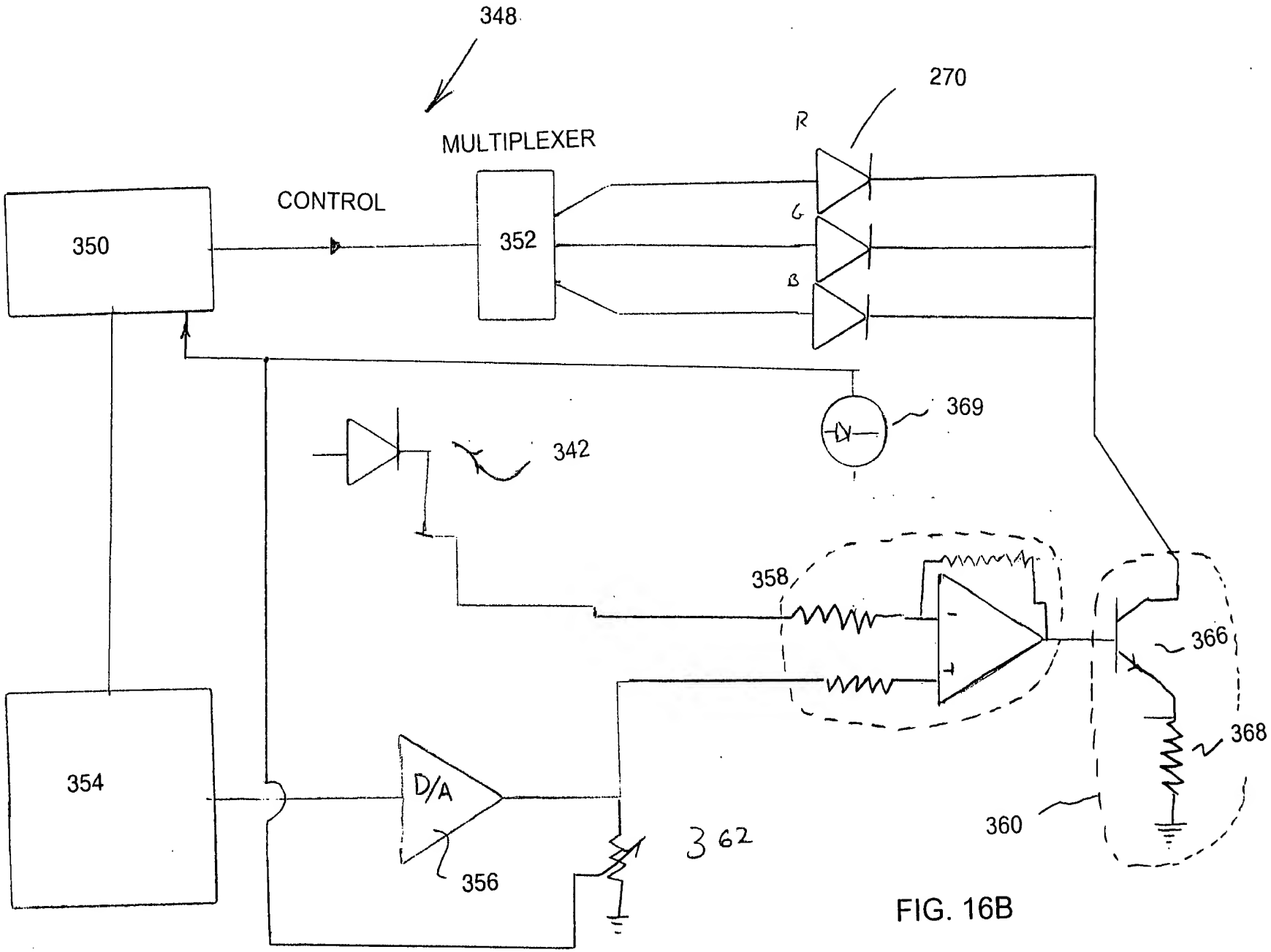

348
MULTIPLEXER
270
R
G
B
CONTROL
350
352
369
342
358
366
368
354
D/A
356
362
360

FIG. 16B

FIG. 17

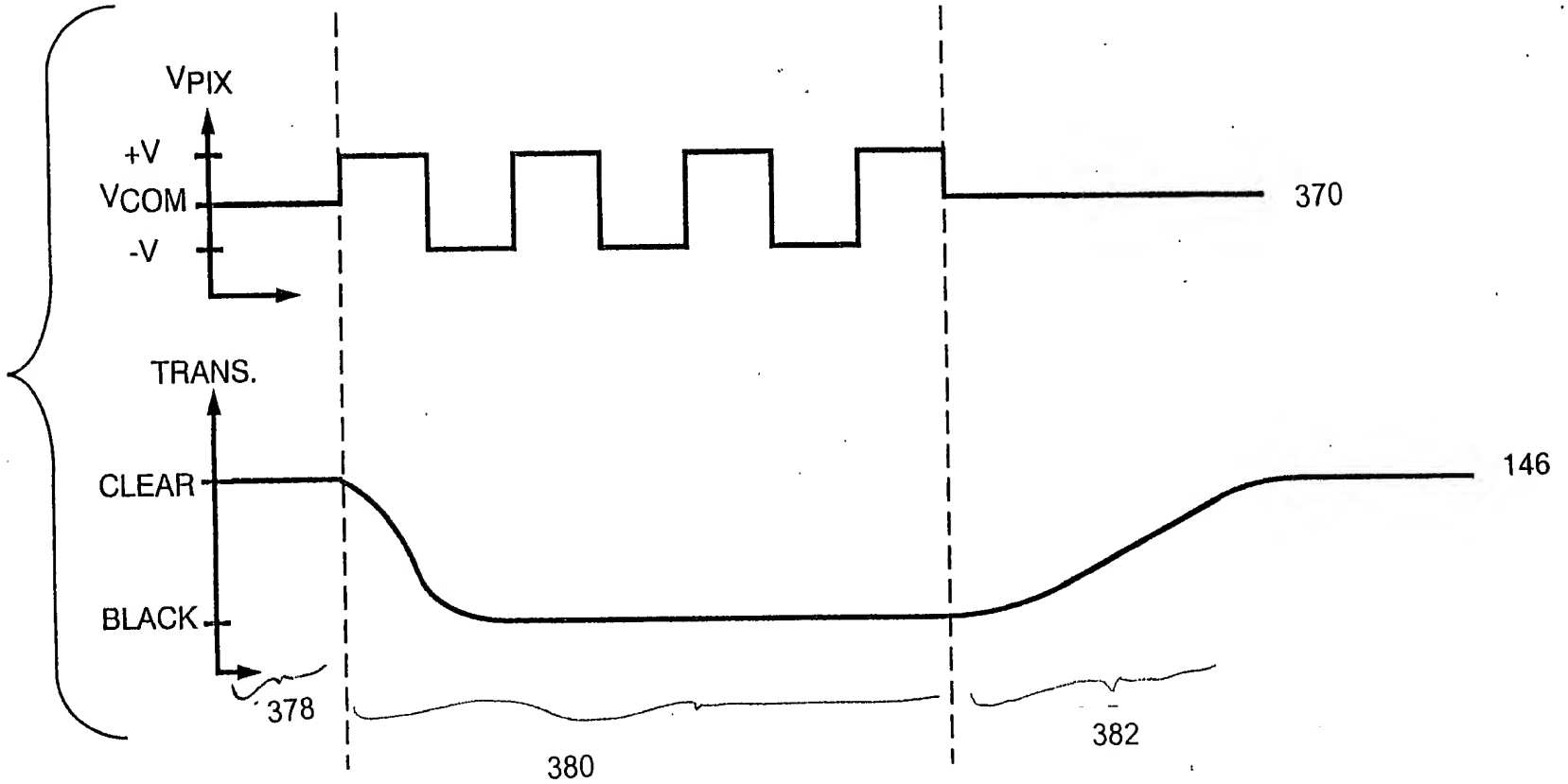
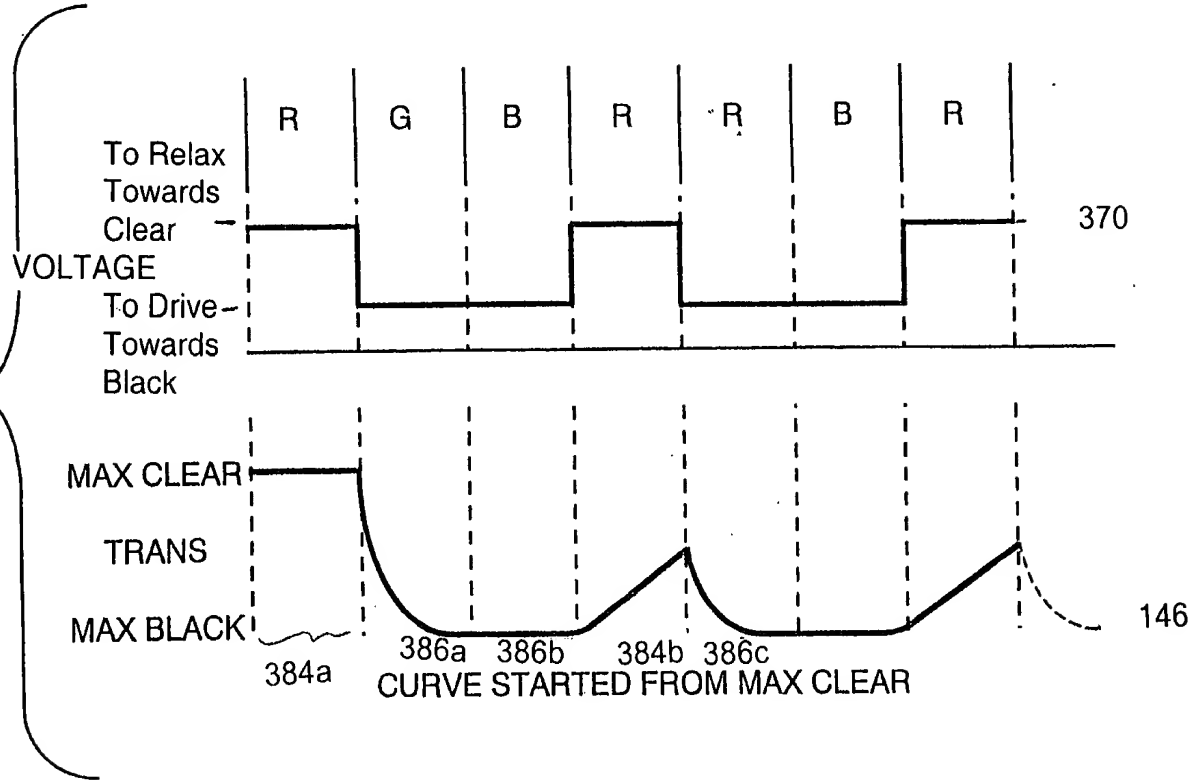


FIG. 18A


R
G
B
R
R
B
R
To Relax Towards Clear
VOLTAGE
To Drive Towards Black
370
MAX CLEAR
TRANS
MAX BLACK
146
384a
386a
386b
384b
386c
CURVE STARTED FROM MAX CLEAR

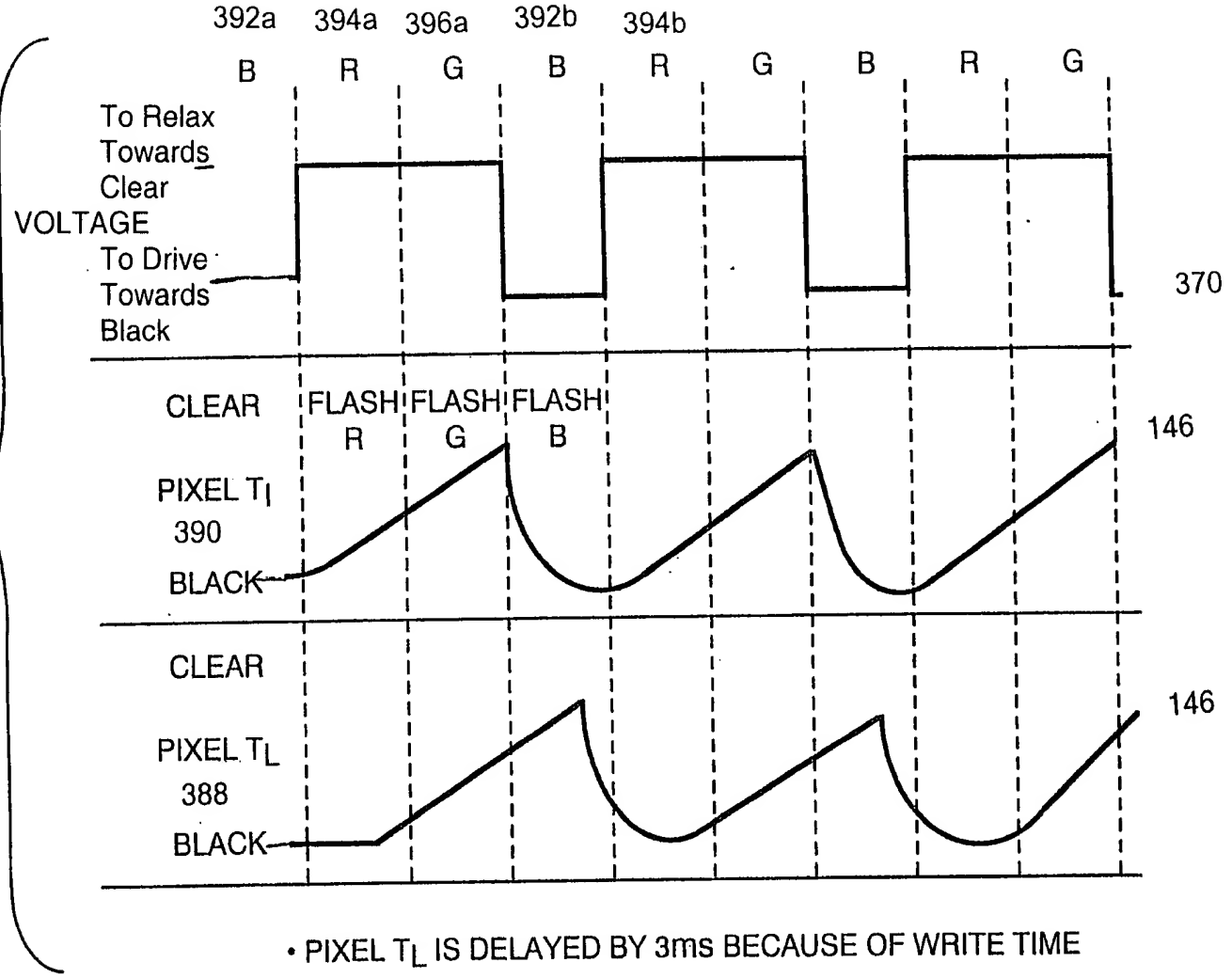


FIG. 18B

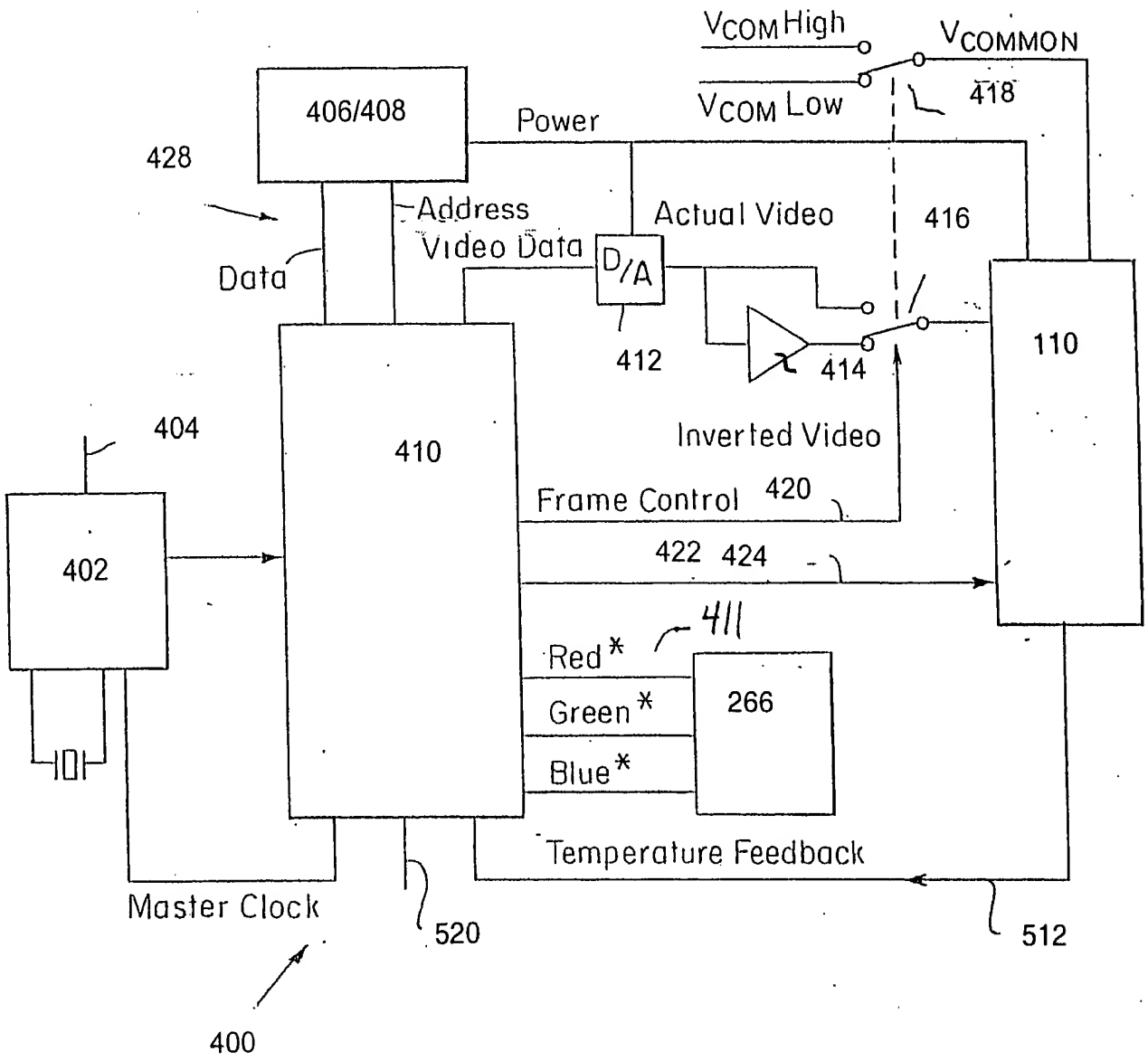


FIG. 19A

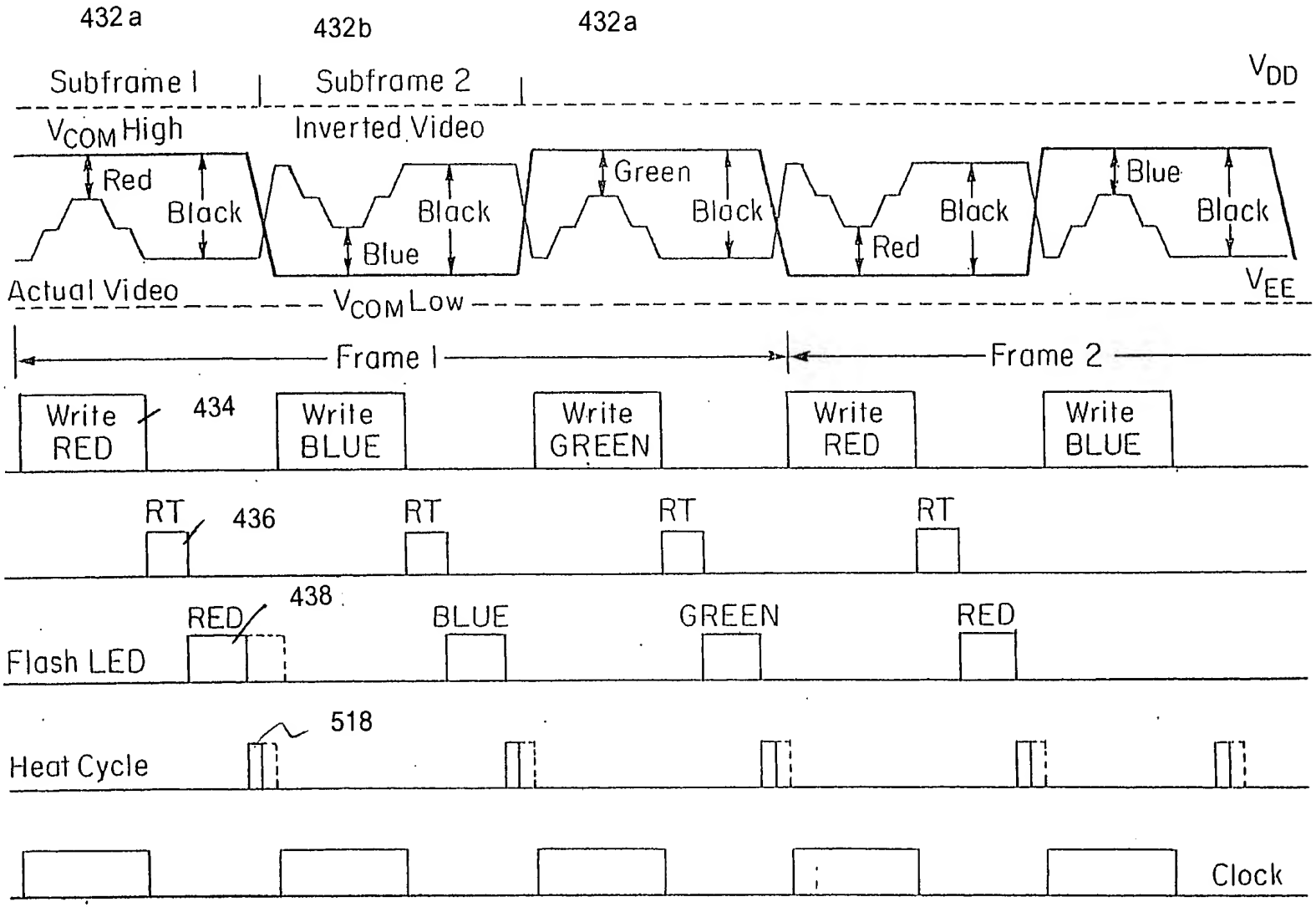

432a
432b
432a
Subframe 1
Subframe 2
V_{DD}
V_{COM} High
Inverted Video
Red
Black
Blue
Green
V_{EE}
Actual Video
V_{COM} Low
Frame 1
Frame 2
Write RED
434
Write BLUE
Write GREEN
RT
436
438
Flash LED
BLUE
GREEN
518
Heat Cycle
Clock

FIG. 19B

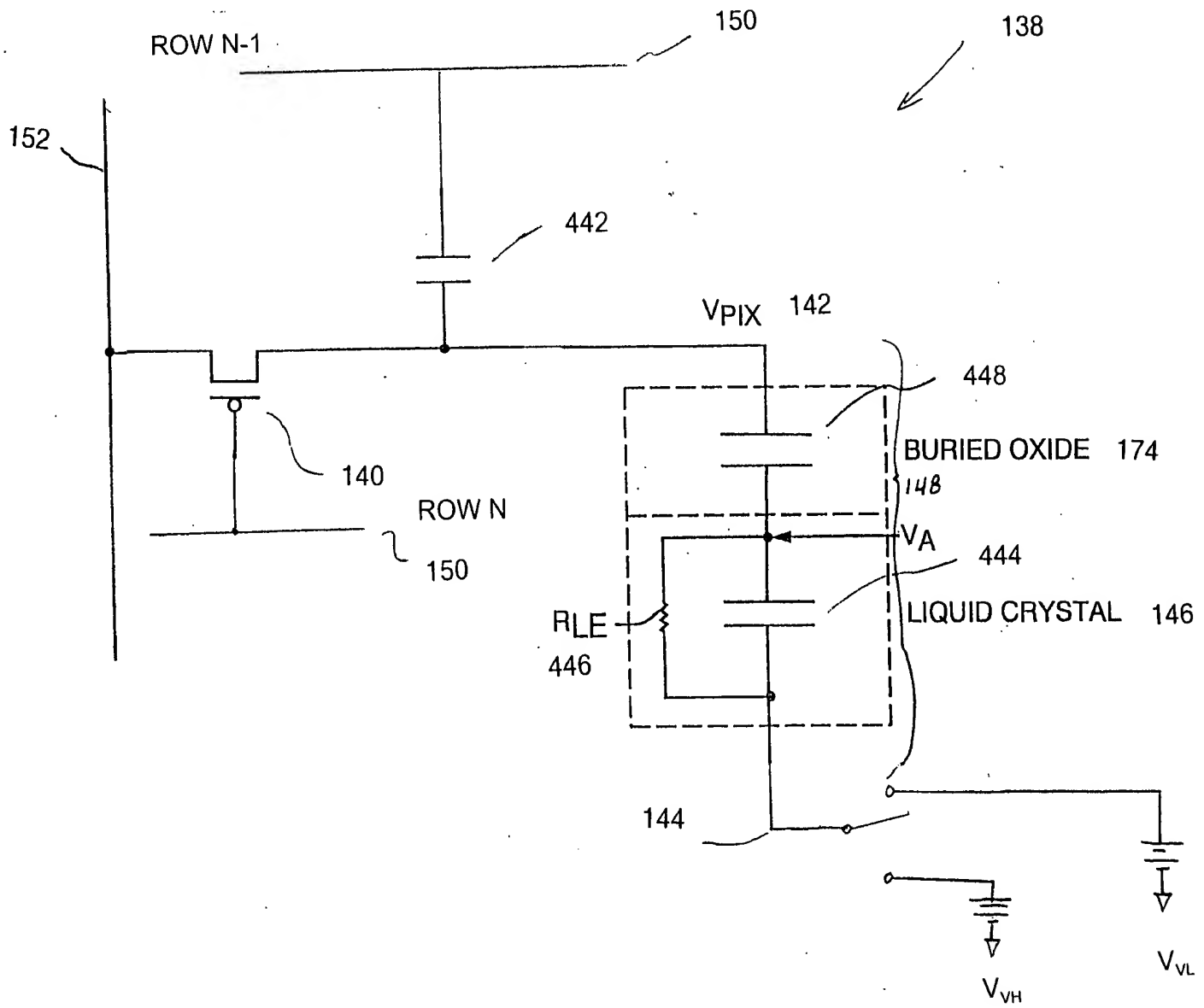


FIG. 20A

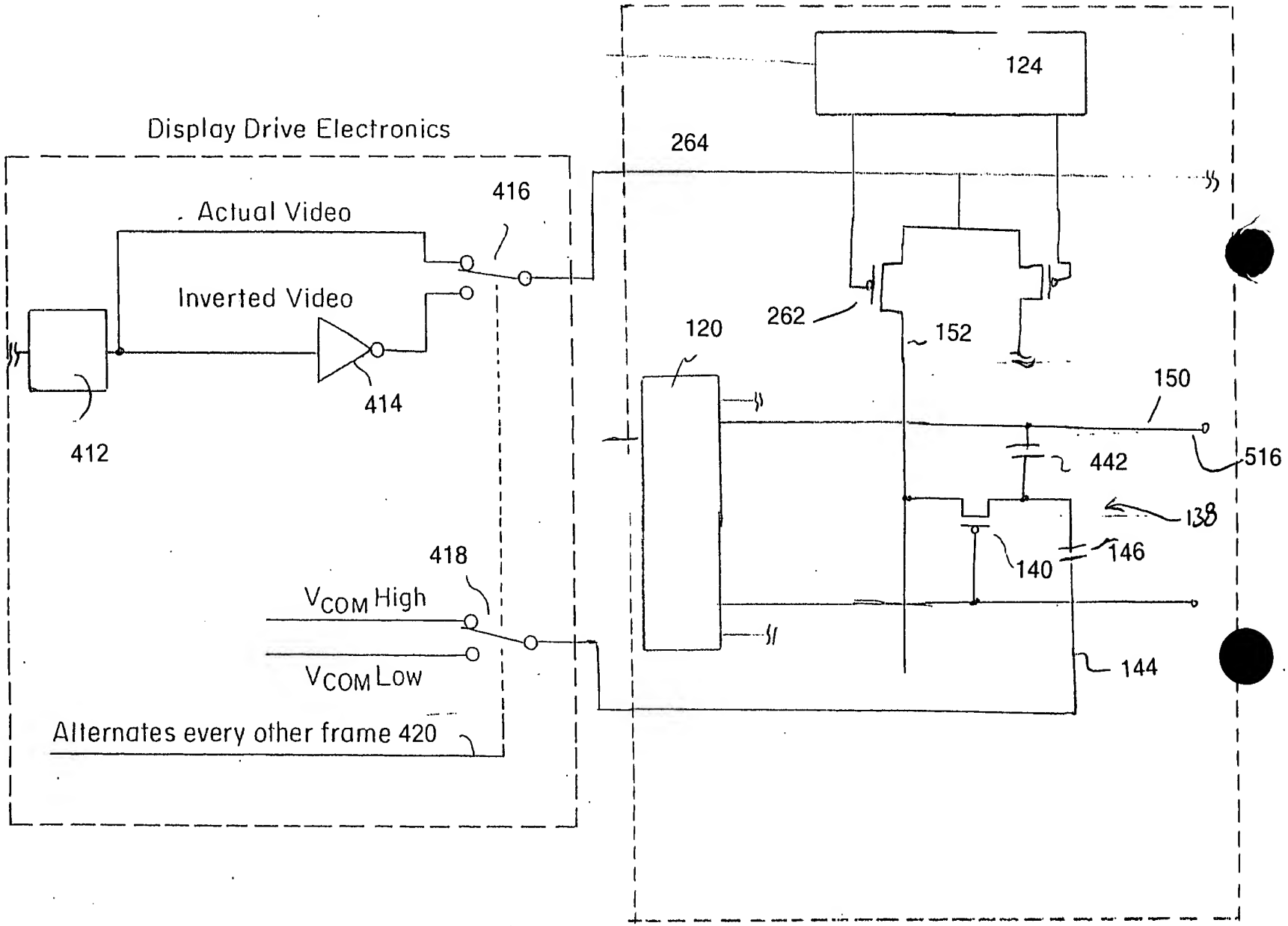

Display Drive Electronics
Actual Video
Inverted Video
416
414
412
418
V_{COM} High
V_{COM} Low
Alternates every other frame 420
264
124
262
152
120
150
442
516
138
140
146
144

FIG. 20B

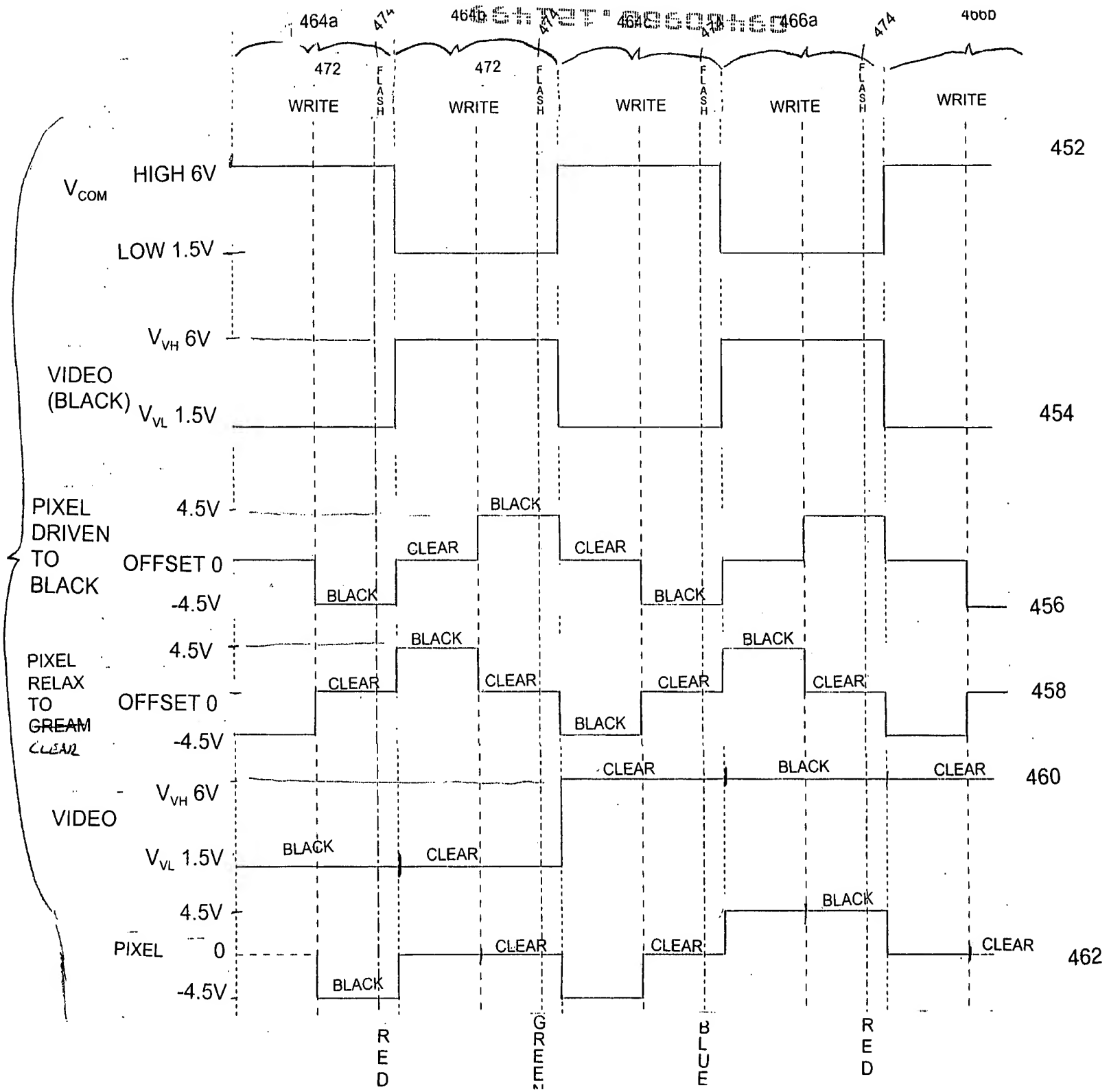

464a
464b
464c
466a
466b
474
472
FLASH
WRITE
V_{COM}
HIGH 6V
LOW 1.5V
V_{VH} 6V
VIDEO (BLACK)
V_{VL} 1.5V
PIXEL DRIVEN TO BLACK
4.5V
OFFSET 0
-4.5V
BLACK
CLEAR
PIXEL RELAX TO GREAM CLEAR
VIDEO
PIXEL
0
RED
GREEN
BLUE
452
454
456
458
460
462

FIG. 21

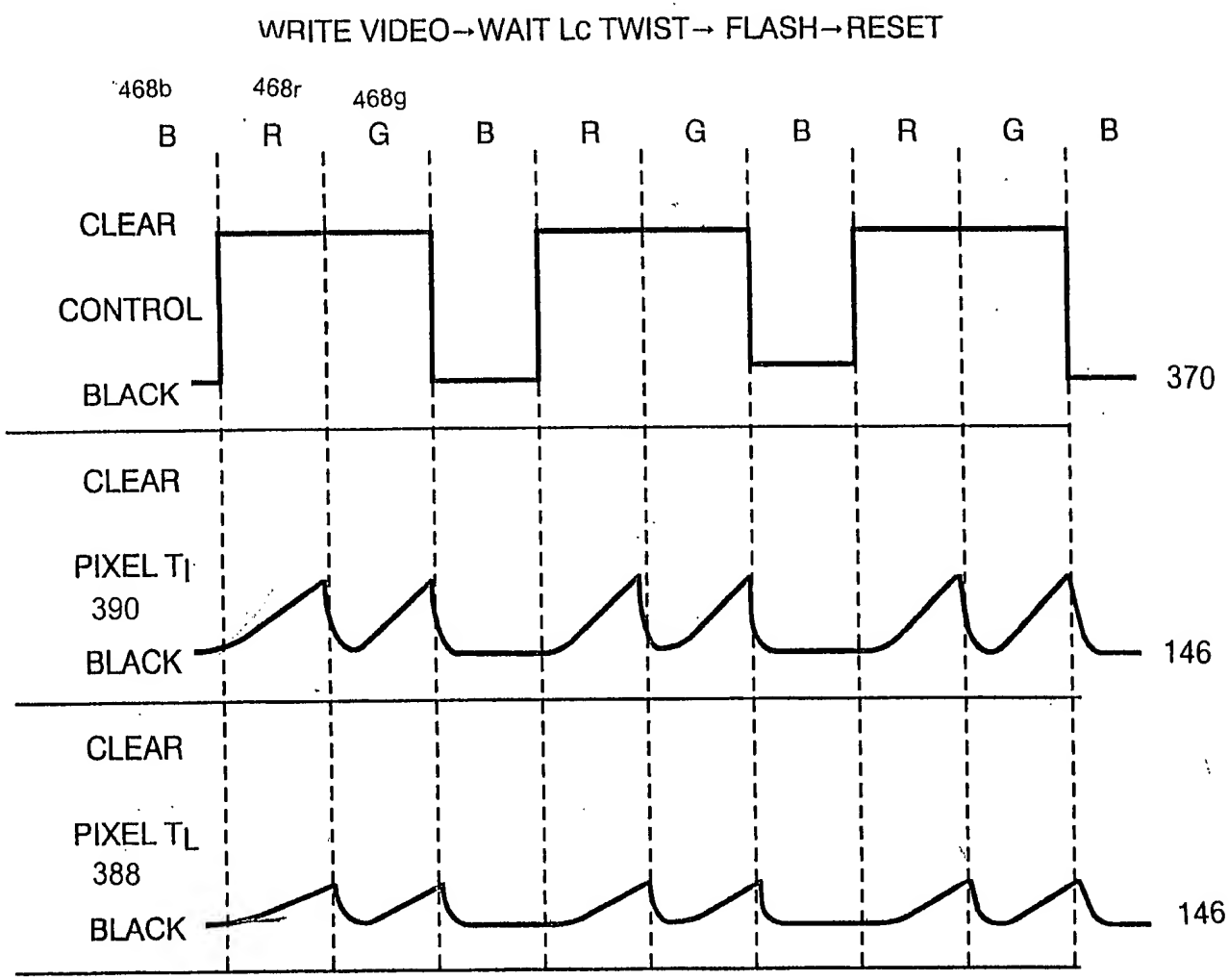

WRITE VIDEO→WAIT Lc TWIST→ FLASH→RESET
468b
468r
468g
B
R
G
B
R
G
B
R
G
B
CLEAR
CONTROL
BLACK
370
CLEAR
PIXEL TI
390
BLACK
146
CLEAR
PIXEL TL
388
BLACK
146

FIG. 22

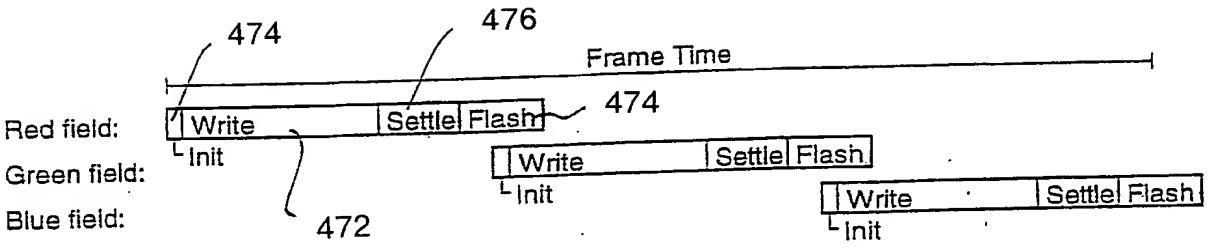


FIG. 23A

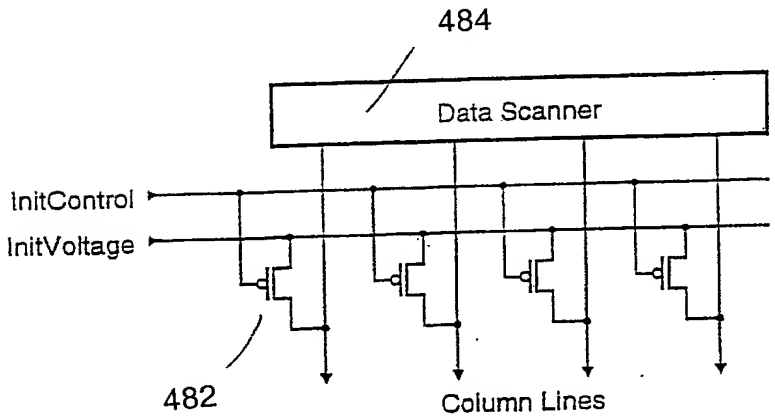


FIG. 23B

FIG. 23C

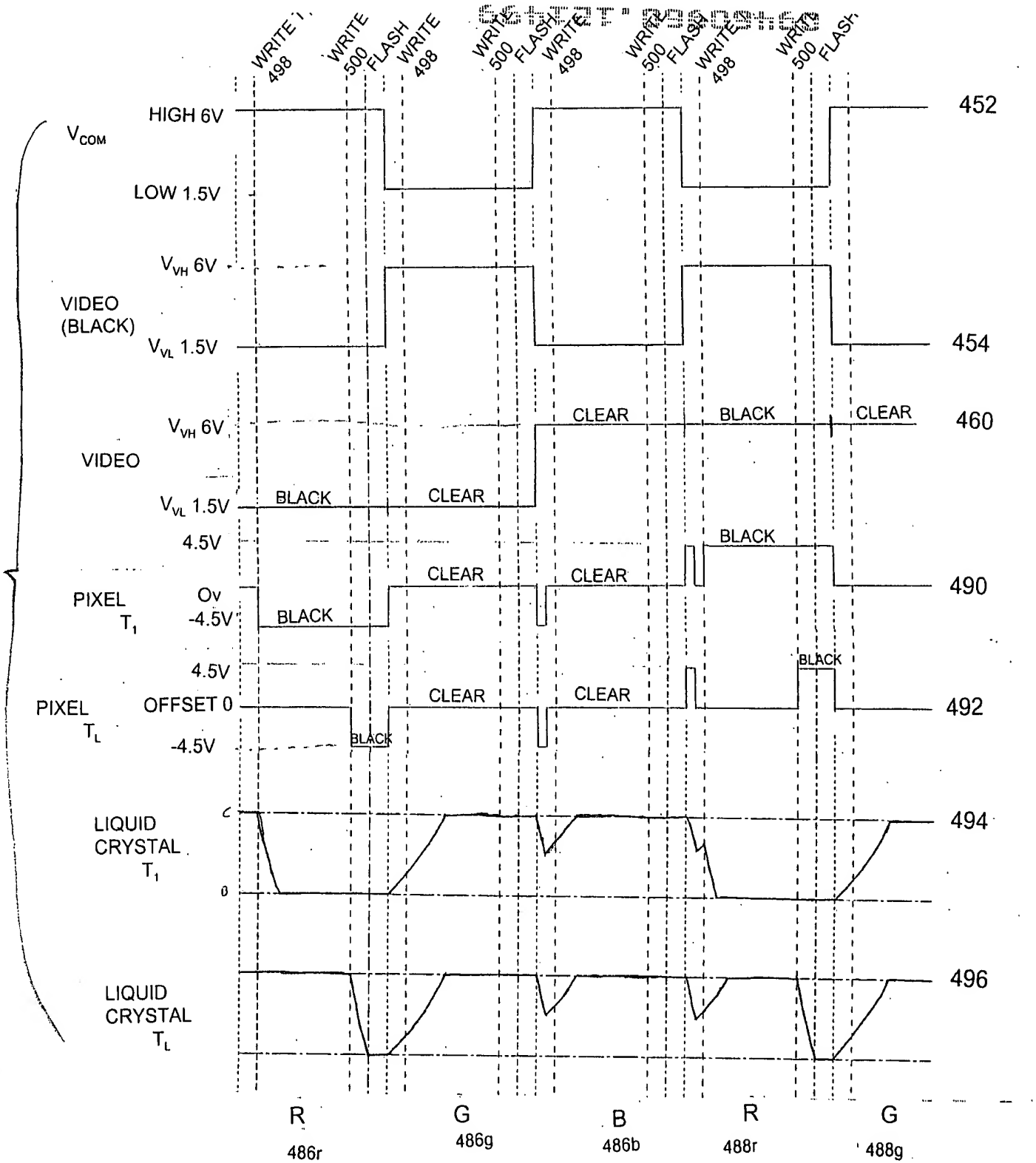
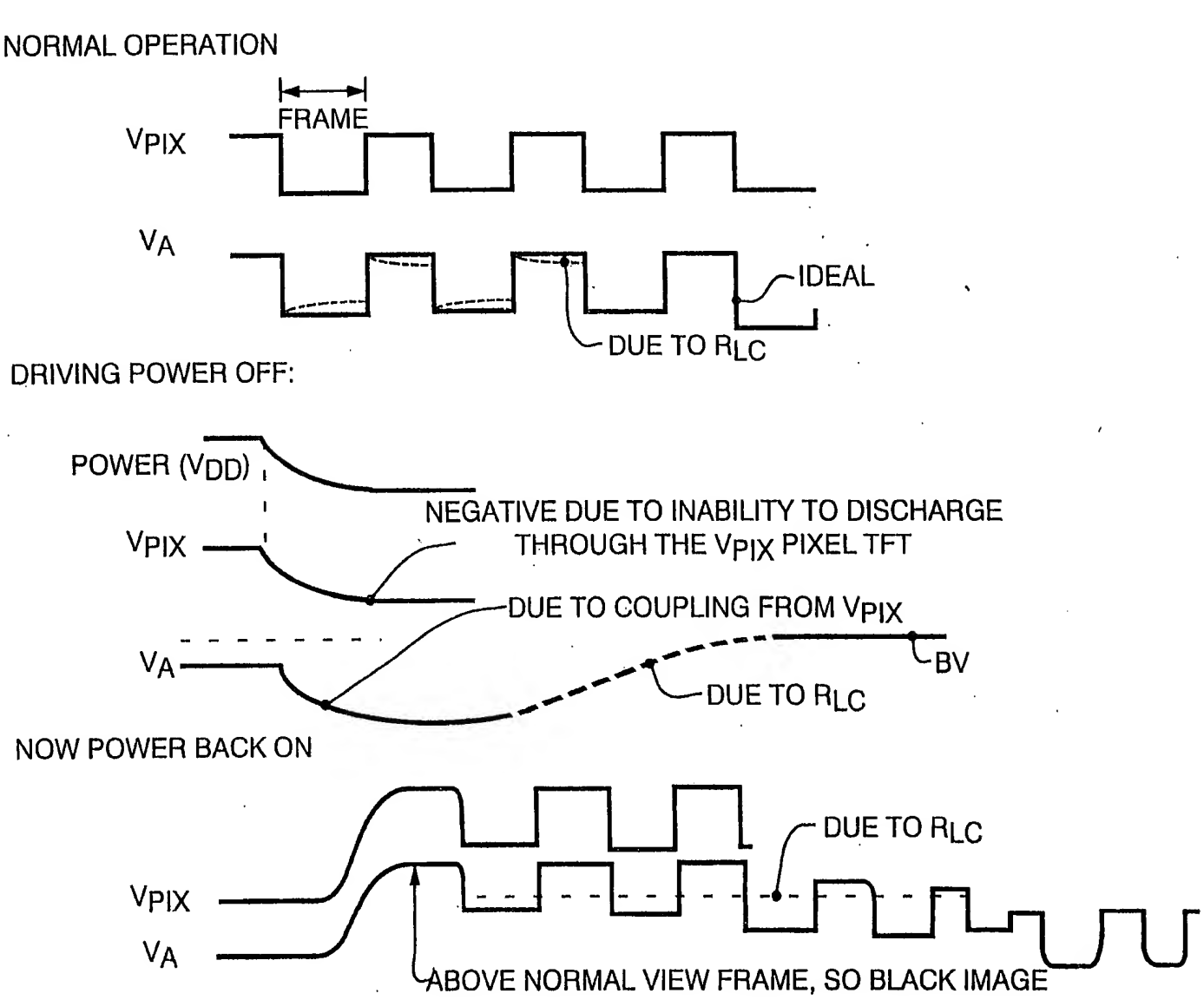

WRITE 498
WRITE 500
FLASH
WRITE 498
WRITE 500
FLASH
WRITE 498
WRITE 500
FLASH
WRITE 498
WRITE 500
FLASH
V_{COM}
HIGH 6V
LOW 1.5V
452
VIDEO (BLACK)
V_{VH} 6V
V_{VL} 1.5V
454
VIDEO
V_{VH} 6V
V_{VL} 1.5V
BLACK
CLEAR
CLEAR
BLACK
CLEAR
460
PIXEL T_1
4.5V
0v
-4.5V
BLACK
CLEAR
CLEAR
BLACK
490
PIXEL T_L
4.5V
OFFSET 0
-4.5V
BLACK
CLEAR
CLEAR
BLACK
492
LIQUID CRYSTAL T_1
494
LIQUID CRYSTAL T_L
496
R
486r
G
486g
B
486b
R
488r
G
488g

FIG. 24



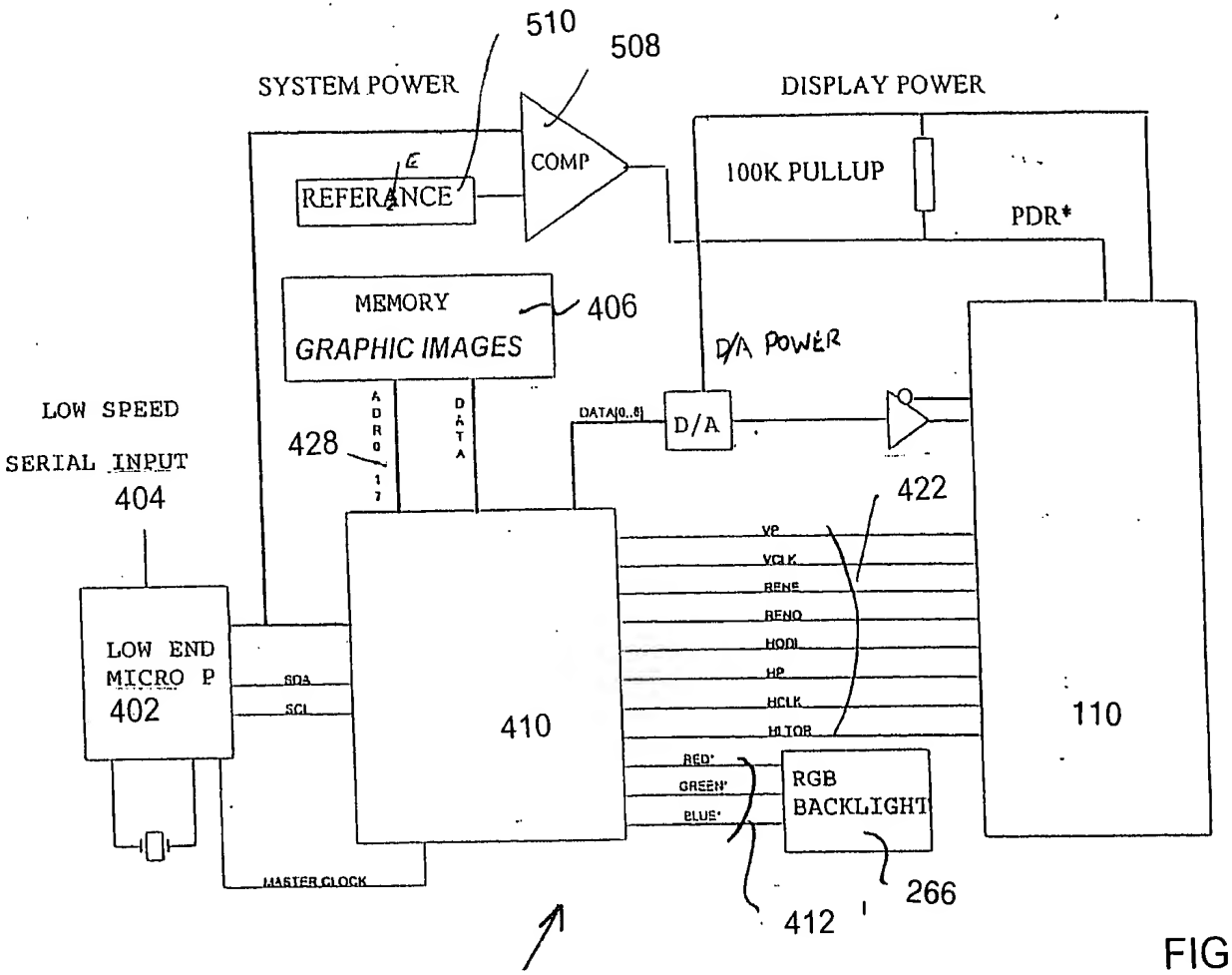

510
508
SYSTEM POWER
DISPLAY POWER
REFERANCE
COMP
100K PULLUP
PDR*
MEMORY
GRAPHIC IMAGES
406
D/A POWER
LOW SPEED
SERIAL INPUT
404
428
ADRO 17
DATA
DATA[0..8]
D/A
422
VP
VCLK
RENE
RENO
HODI
HP
HCLK
HITOR
LOW END
MICRO P
402
SDA
SCL
410
110
RED*
GREEN*
BLUE*
RGB
BACKLIGHT
MASTER CLOCK
412
266
506

FIG. 25

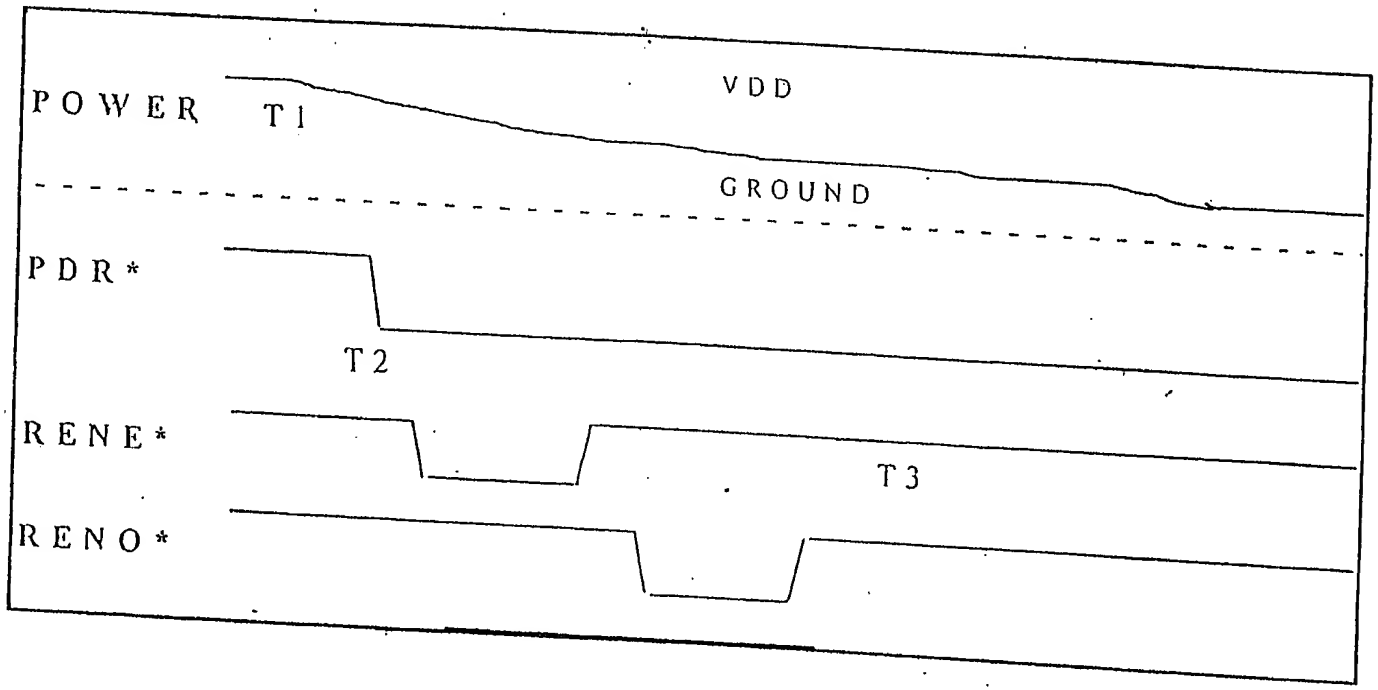


FIG. 26

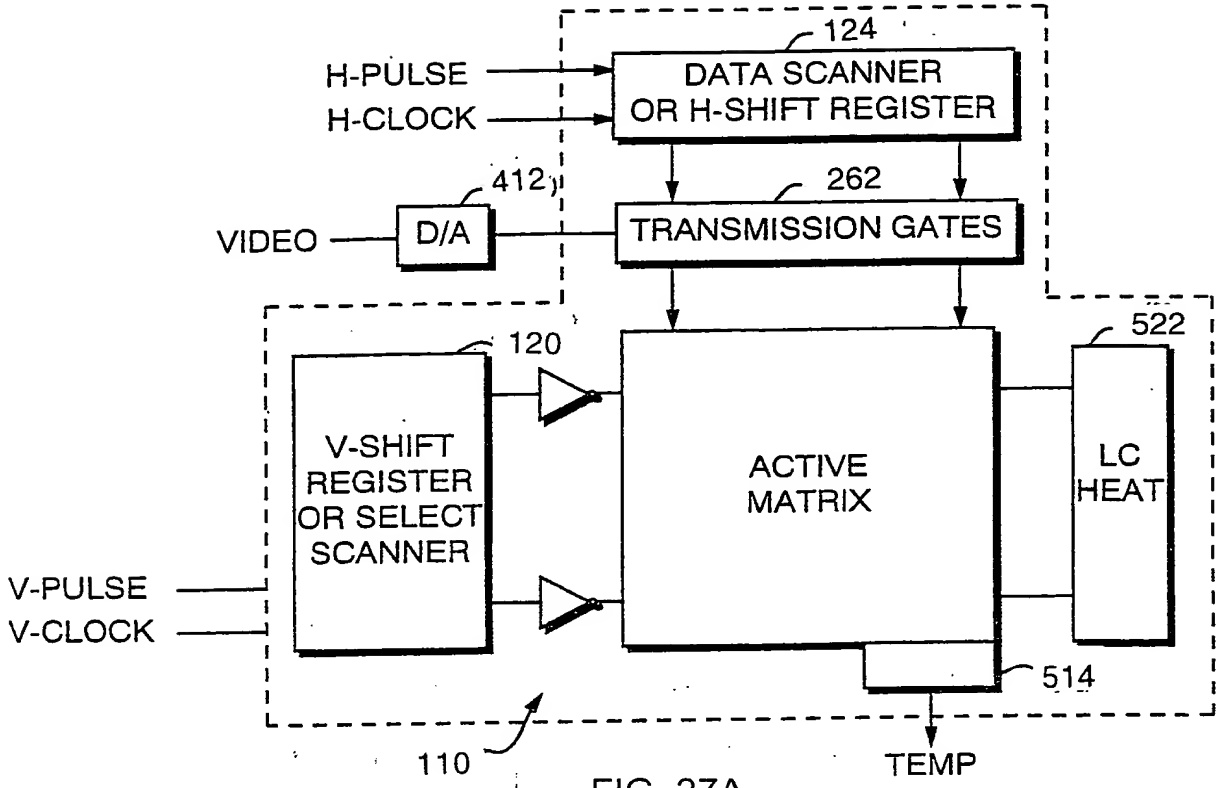


FIG. 27A

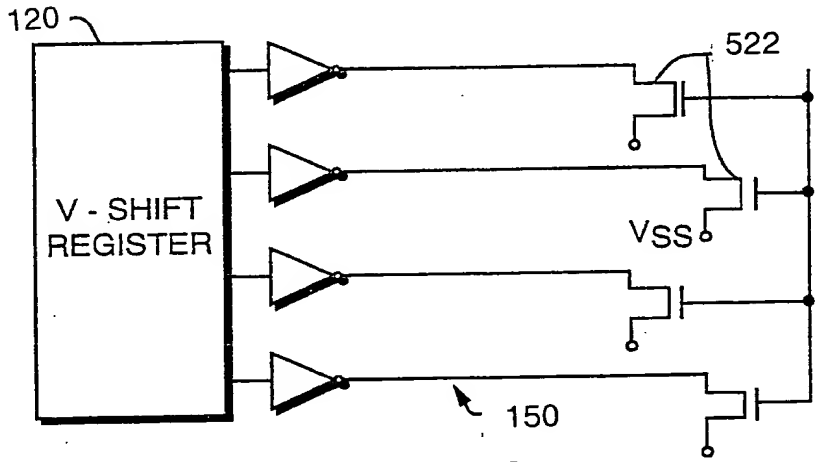


FIG. 27B

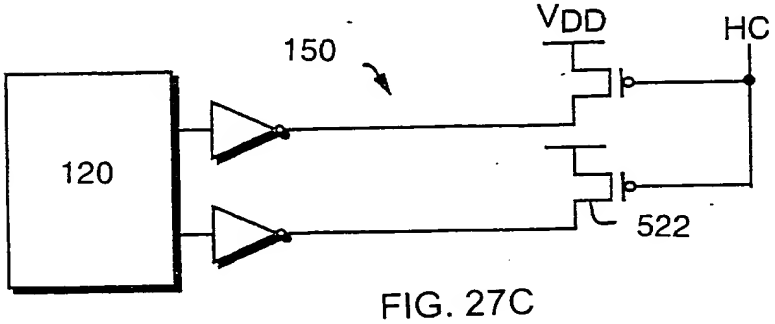


FIG. 27C

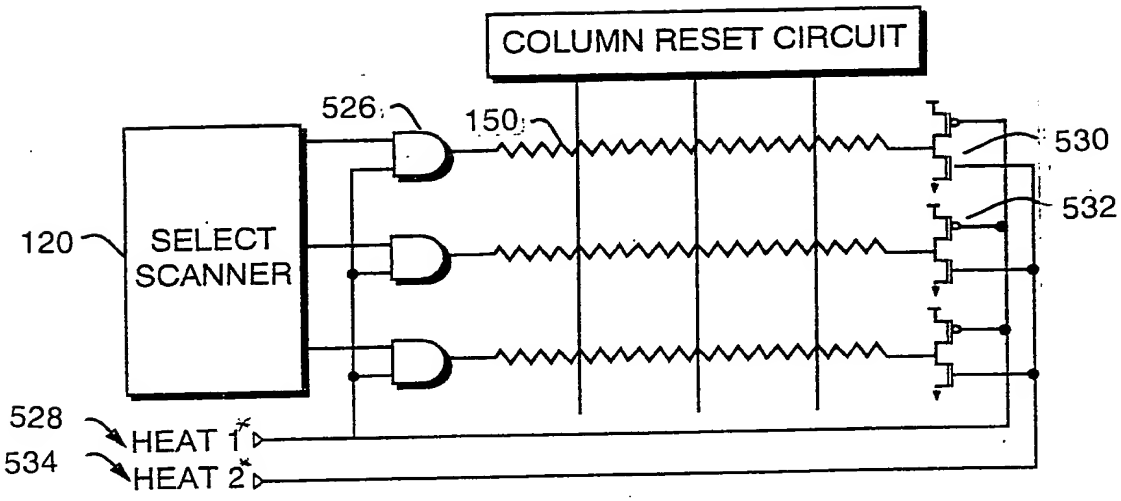


FIG. 27D

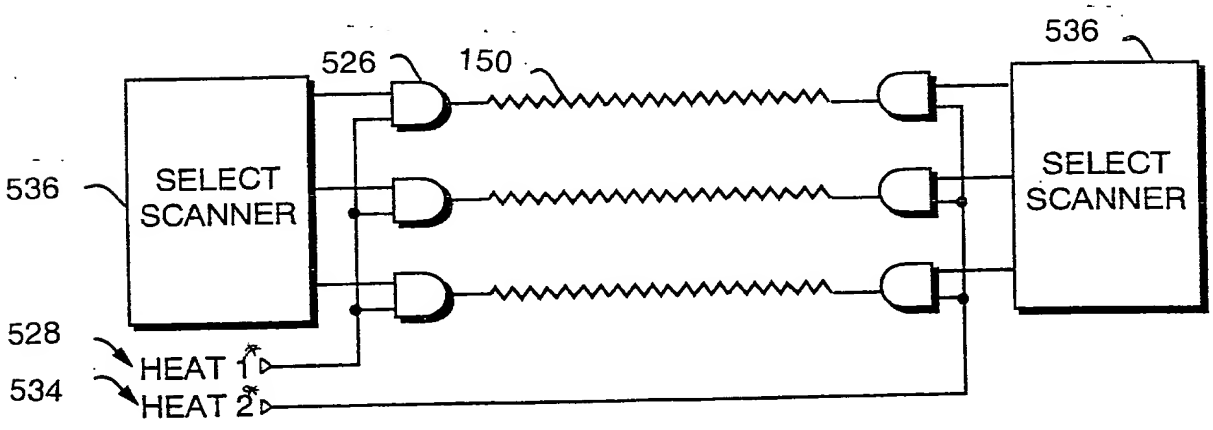


FIG. 27E

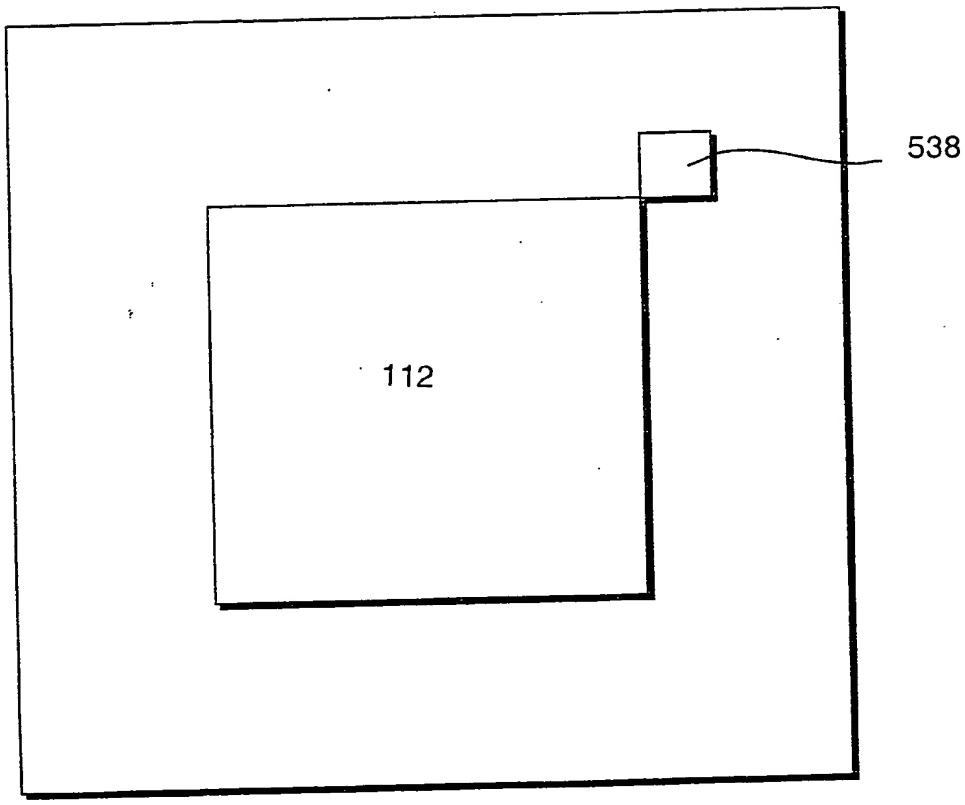


FIG. 27F

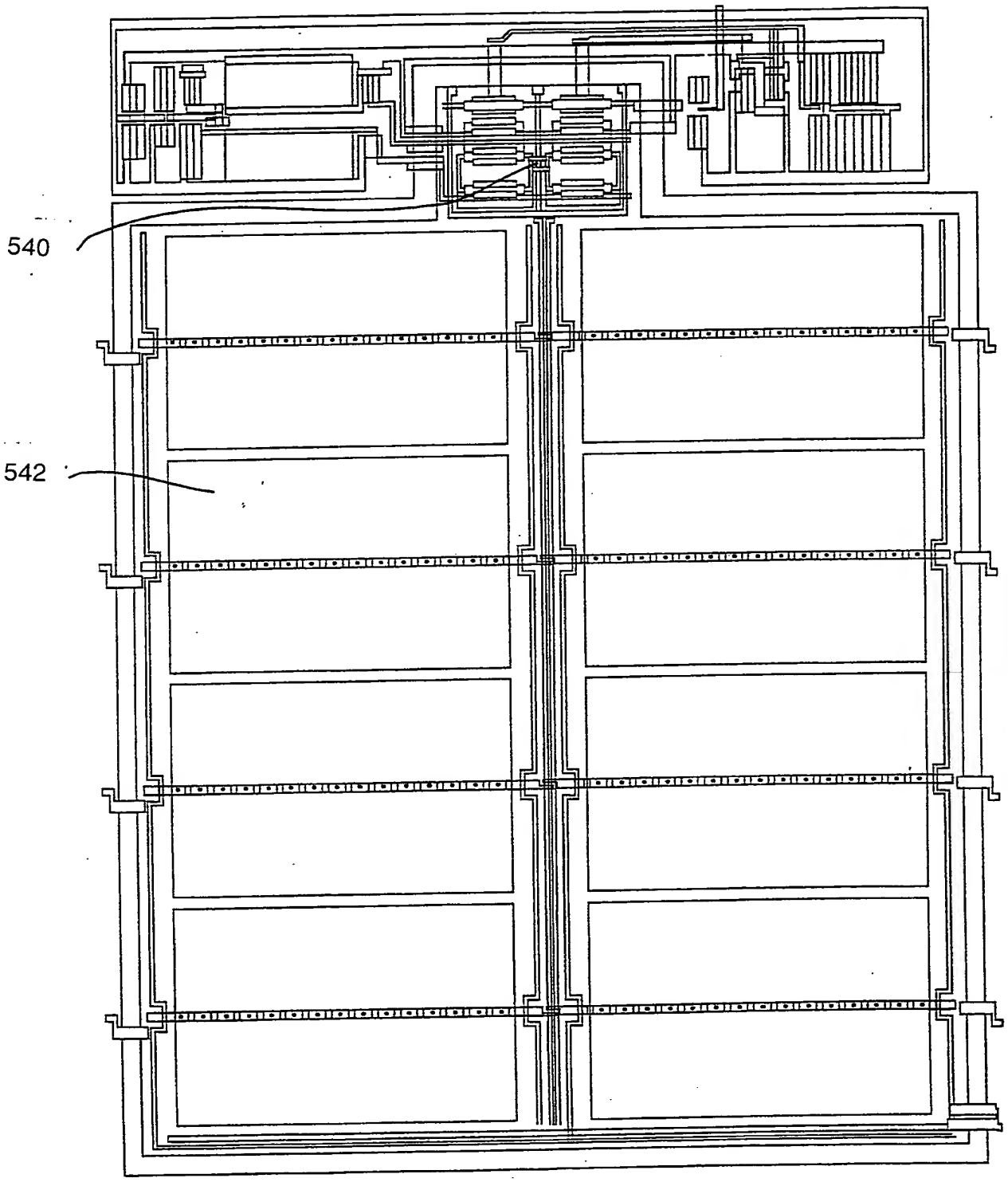


FIG. 27G

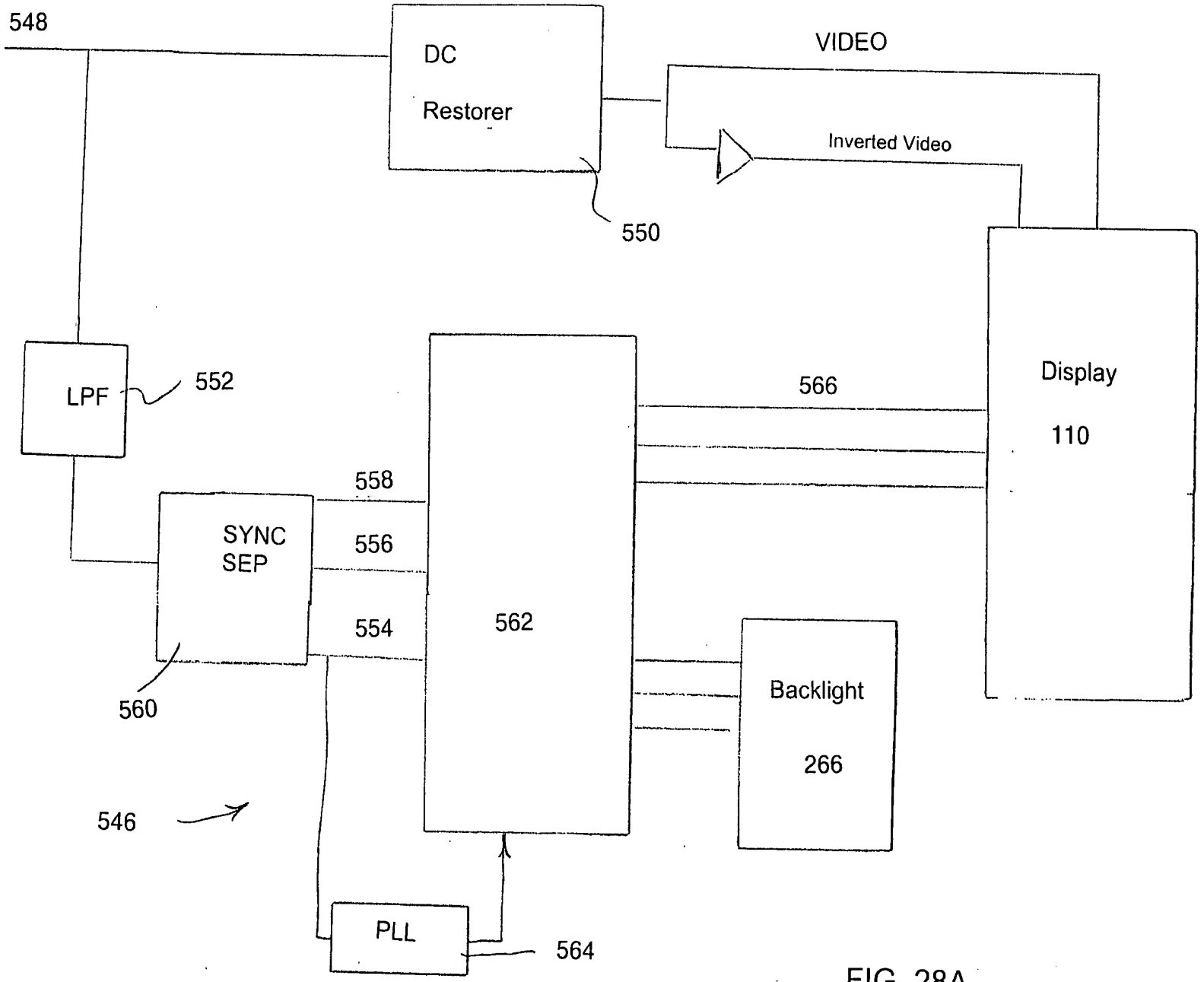


FIG. 28A

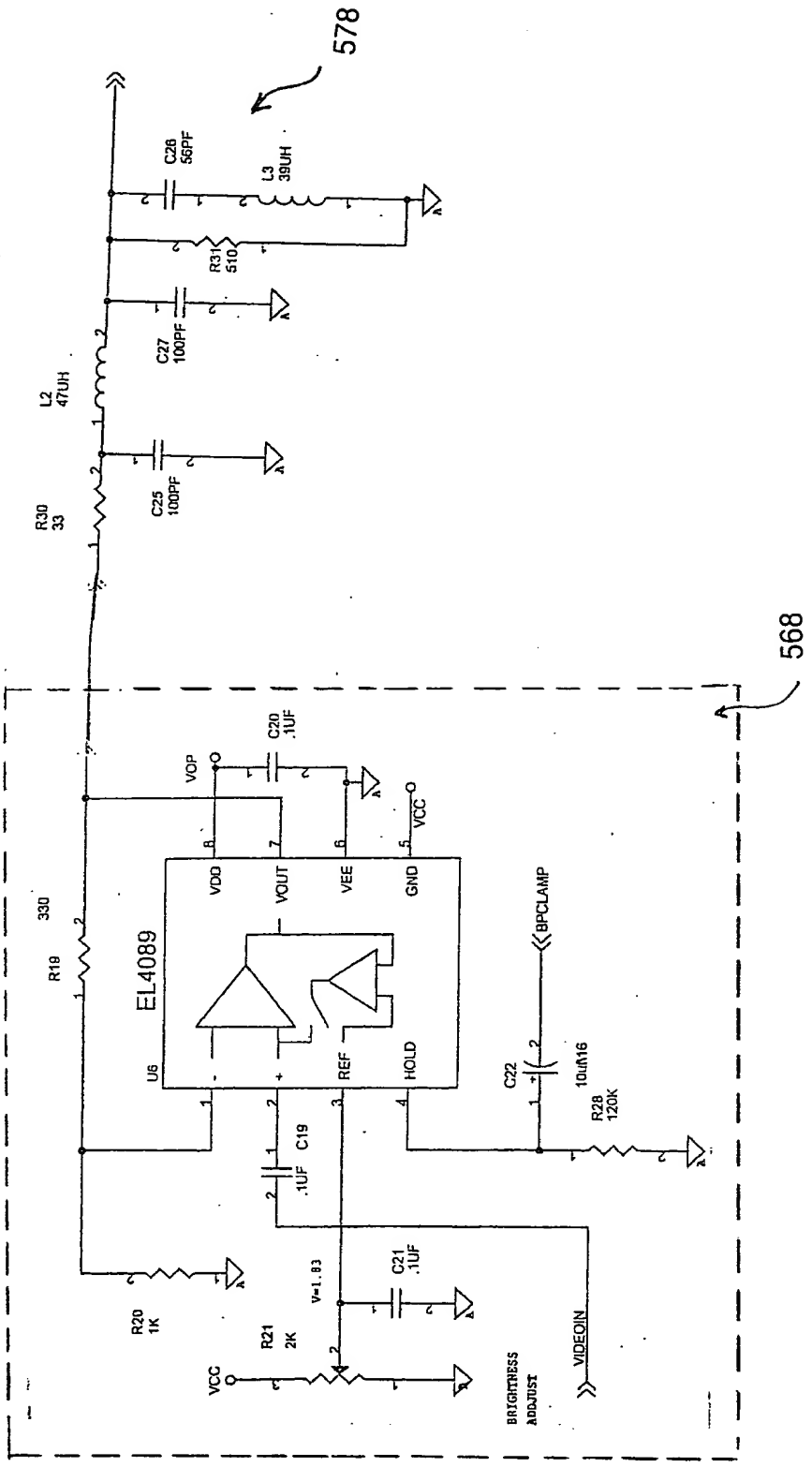

578
568
C26
56PF
L3
39UH
R31
510
C27
100PF
L2
47UH
C25
100PF
R30
33
C20
.1UF
VOP
VCC
VDD
VOUT
VEE
GND
EL4089
U6
REF
HOLD
R19
330
BPCLAMP
C22
10uM16
R28
120K
C19
.1UF
C21
.1UF
V=1.83
R20
1K
R21
2K
VCC
BRIGHTNESS
ADJUST
VIDEOIN

FIG. 28B

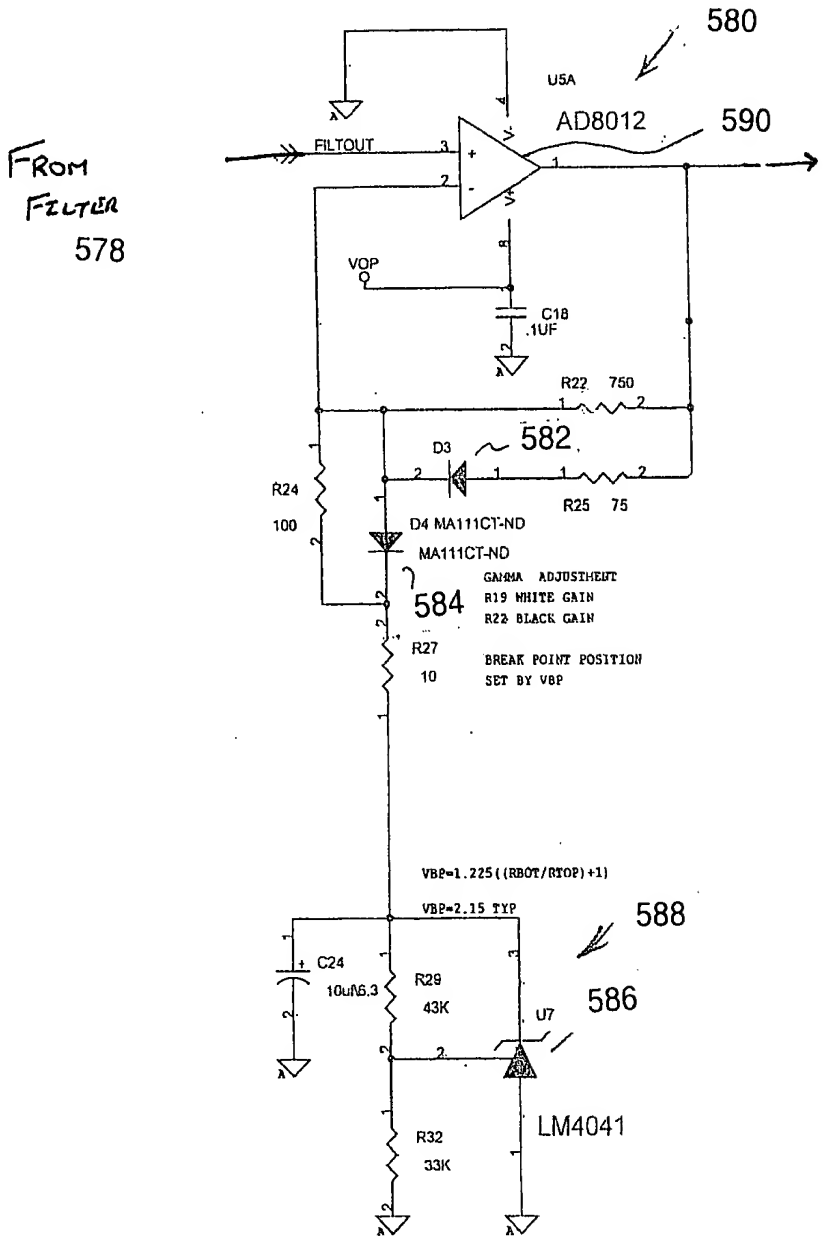

580
U5A
AD8012
590
FILTOUT
FROM FILTER 578
TO DISPLAY
VOP
C18
.1UF
R22 750
582
D3
R25 75
R24
100
D4 MA111CT-ND
MA111CT-ND
GAMMA ADJUSTMENT
R19 WHITE GAIN
R22 BLACK GAIN
584
R27
10
BREAK POINT POSITION
SET BY VBP
VBP=1.225((RBOT/RTOP)+1)
VBP=2.15 TYP
588
C24
10uF6.3
R29
43K
U7
586
LM4041
R32
33K

FIG. 28C

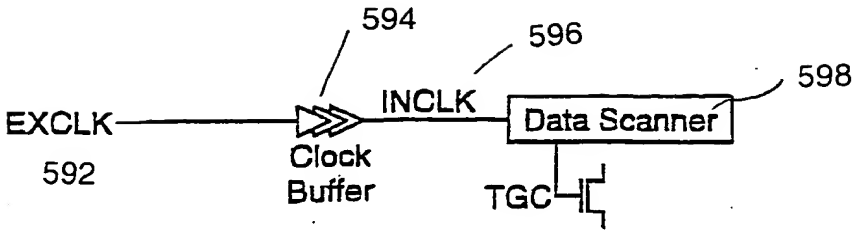


FIG. 29A

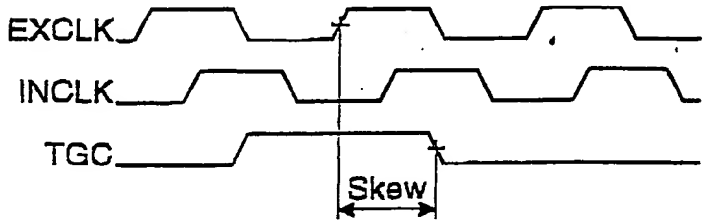


FIG. 29B

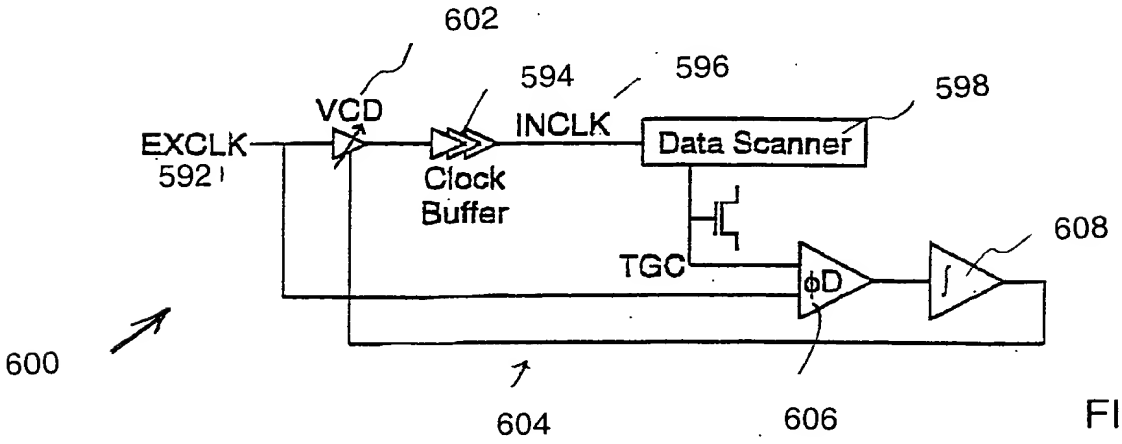


FIG. 29C

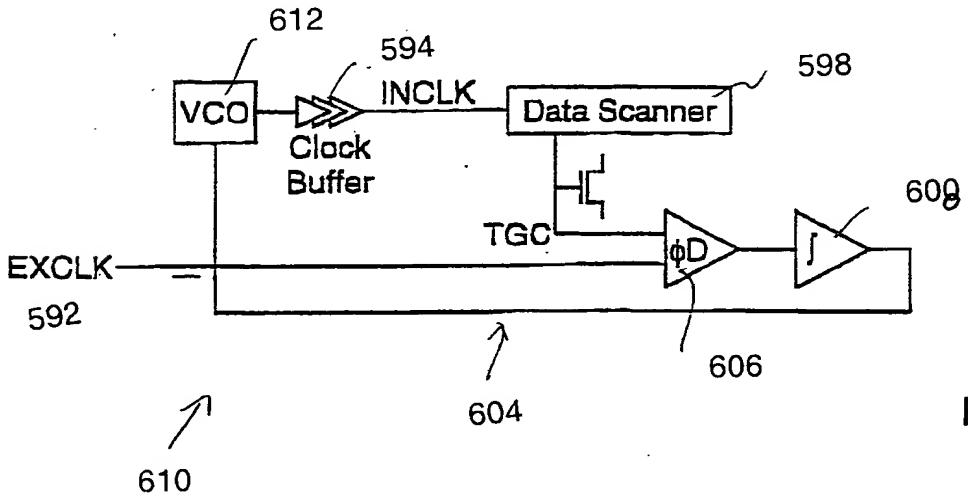


FIG. 29D

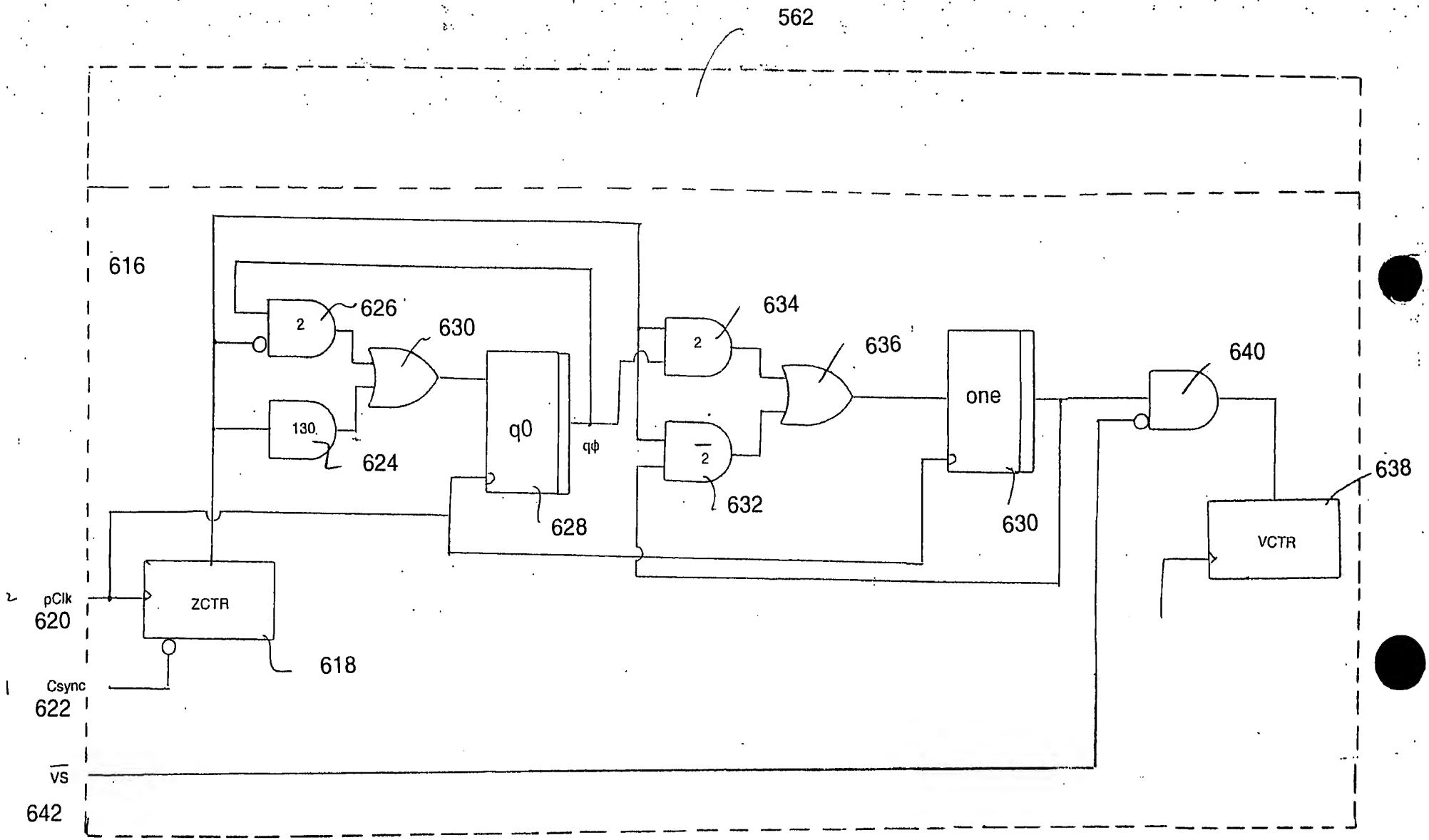


FIG. 30

MORE

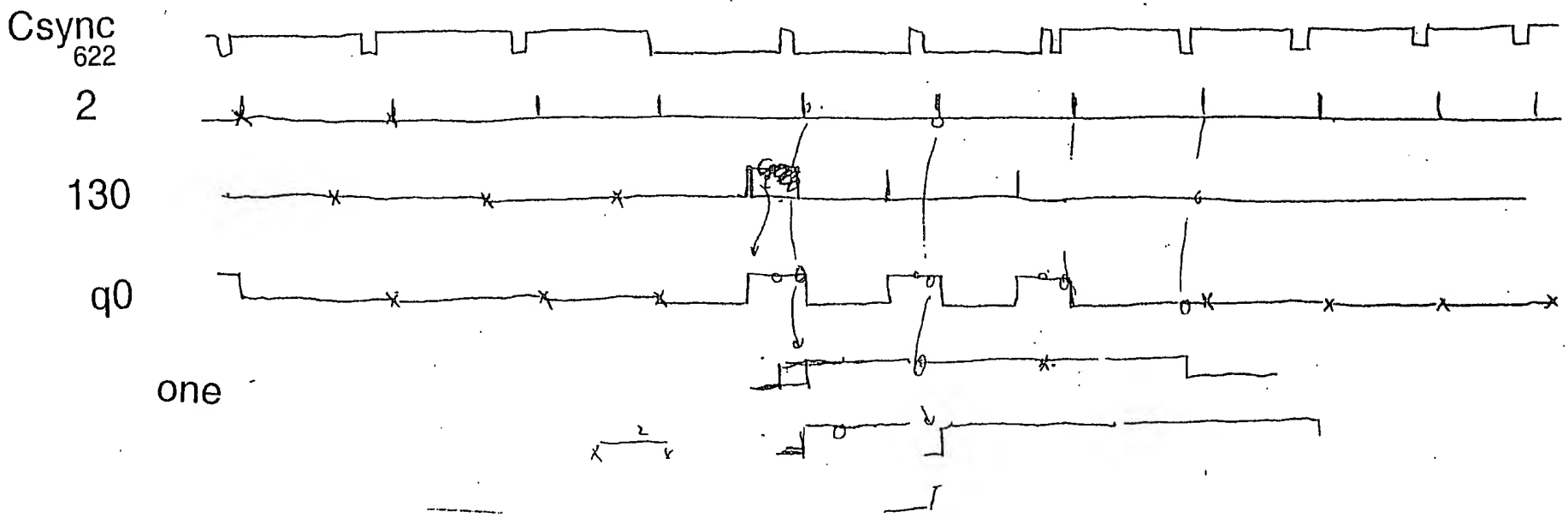


FIG. 31.

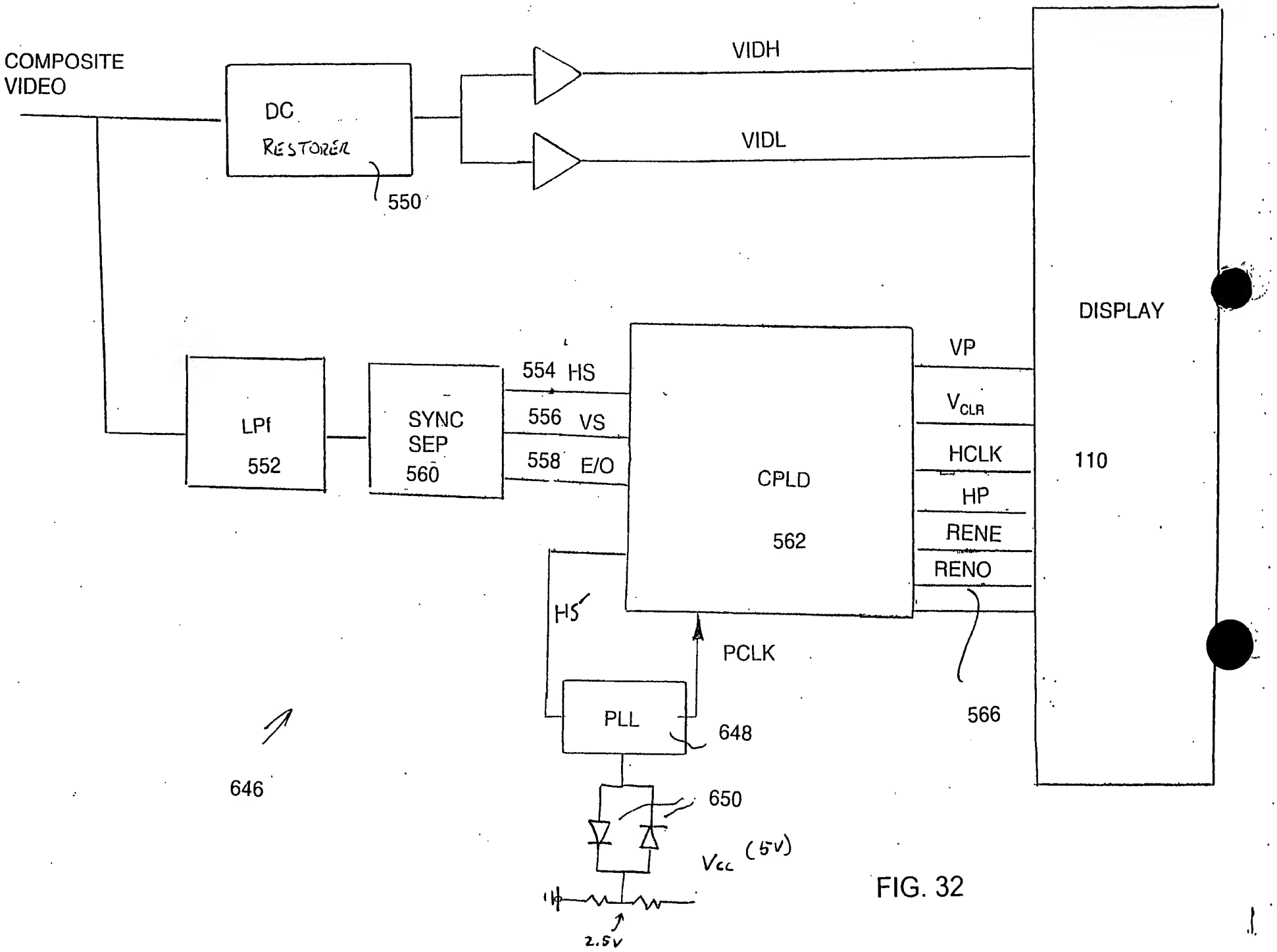

COMPOSITE VIDEO
DC RESTORER
550
VIDH
VIDL
DISPLAY
110
LPf
552
SYNC SEP
560
554 HS
556 VS
558 E/O
CPLD
562
VP
V_{CLR}
HCLK
HP
RENE
RENO
566
HS
PCLK
PLL
648
646
650
V_{cc} (5V)
2.5V

FIG. 32

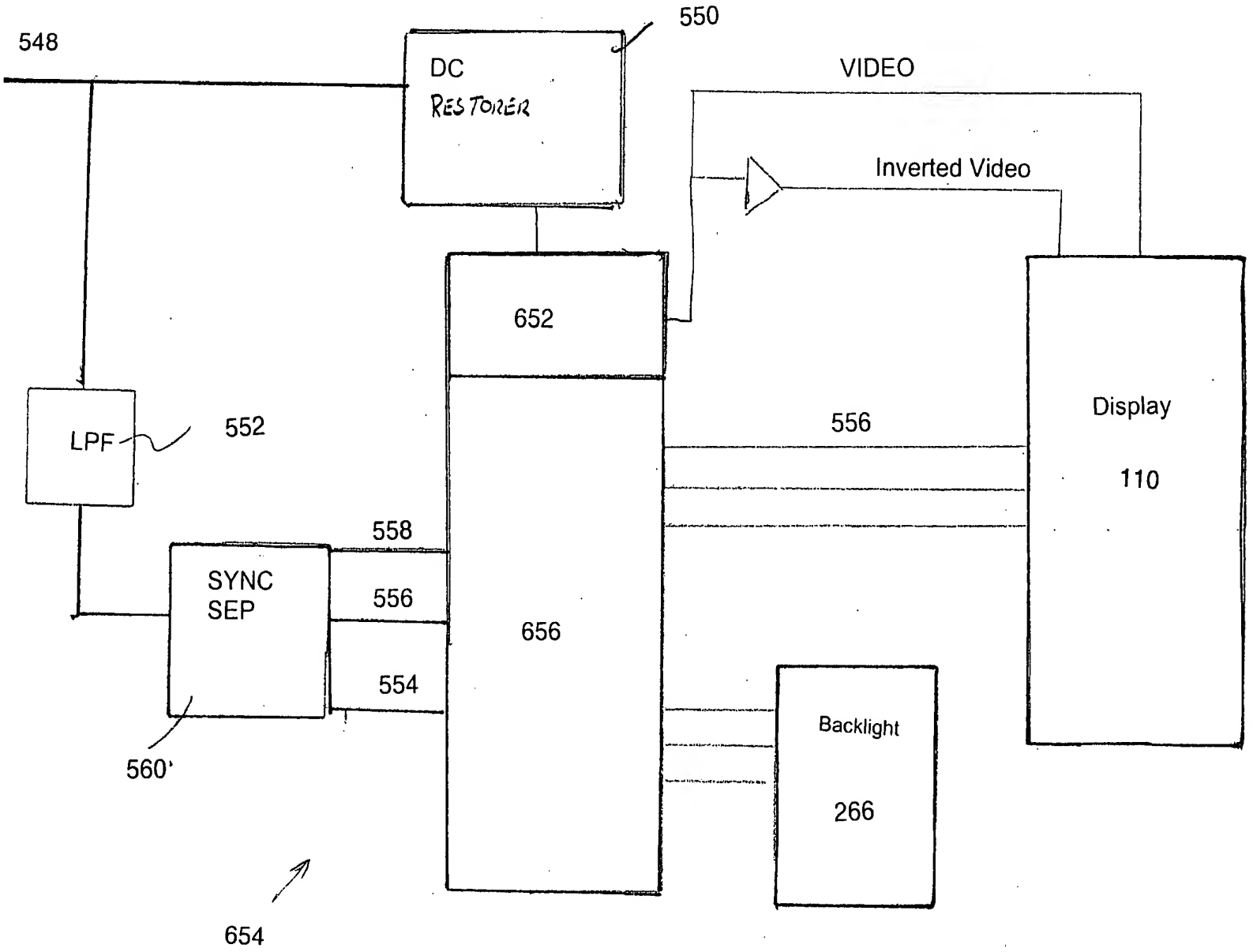
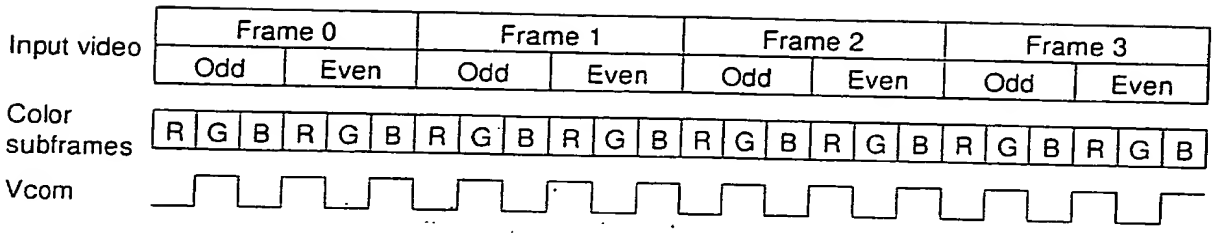


FIG. 33



Timing diagram with 3:1 ratio of subframes to fields

FIG. 34A

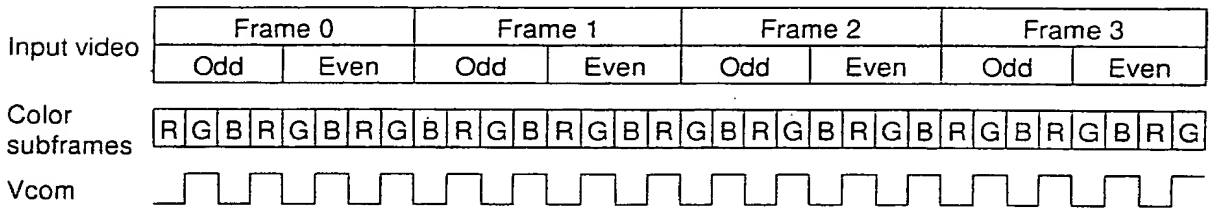


FIG. 34B Timing diagram with 4:1 ratio of subframes to fields

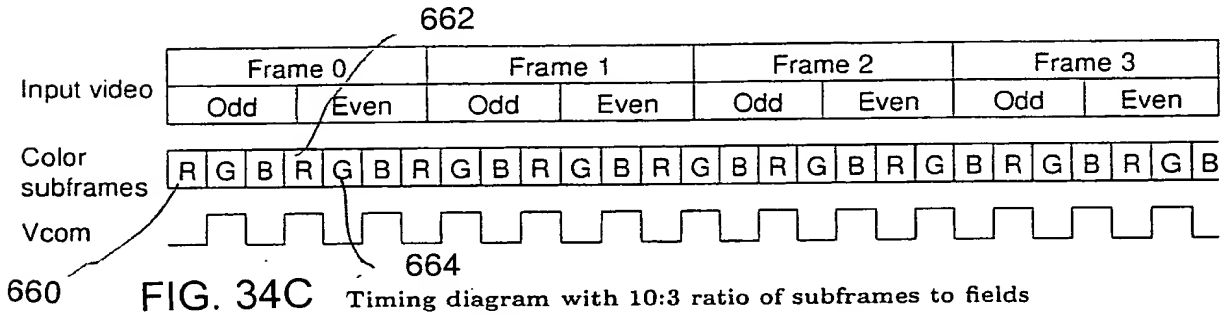


FIG. 34C Timing diagram with 10:3 ratio of subframes to fields

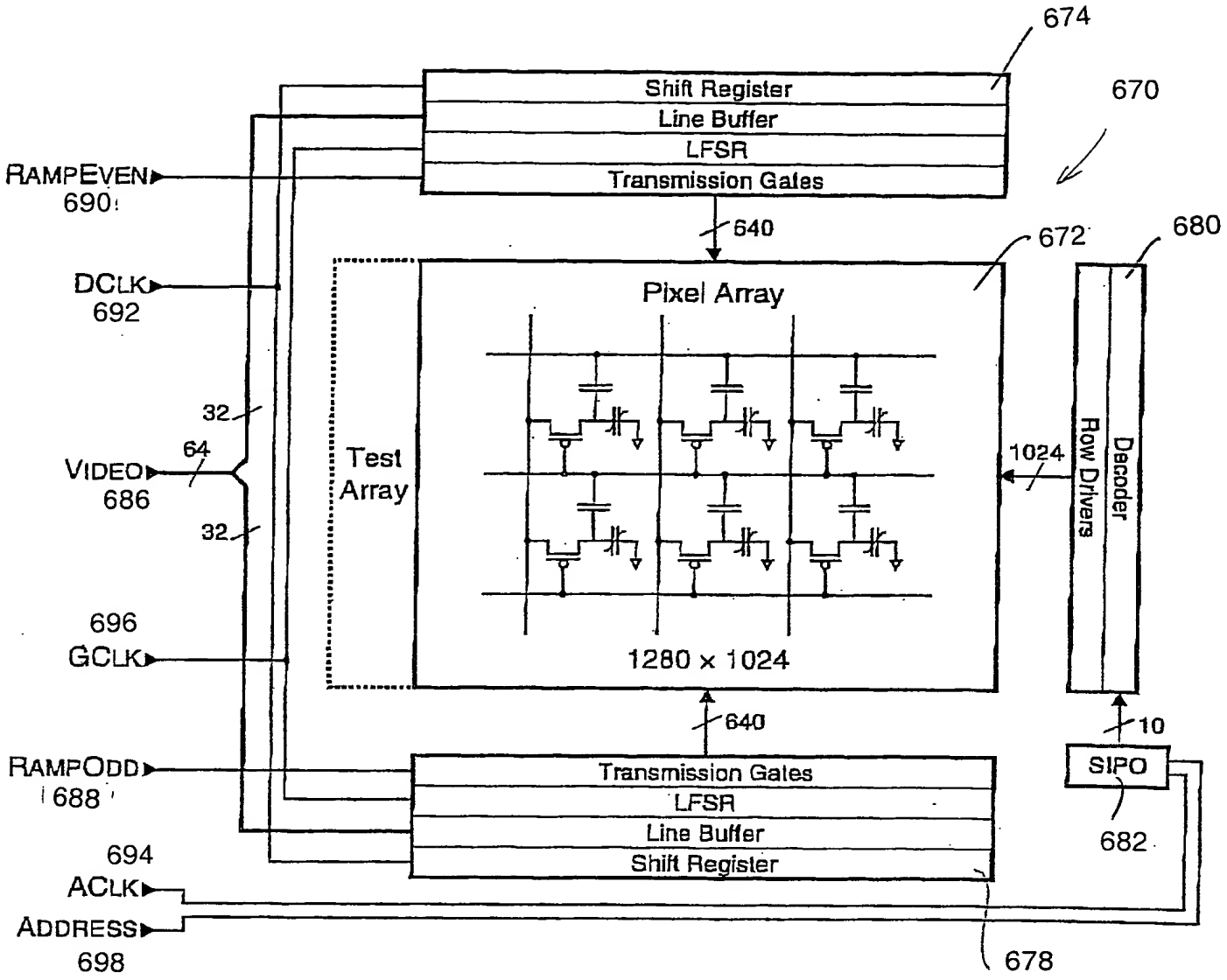

674
Shift Register
Line Buffer
LFSR
Transmission Gates
670
RAMPEVEN
690
640
672
680
DCLK
692
Pixel Array
32
64
VIDEO
686
32
Test
Array
1024
Row Drivers
Decoder
696
GCLK
1280 x 1024
640
10
RAMPODD
688
Transmission Gates
LFSR
Line Buffer
Shift Register
SIPO
682
694
ACLK
ADDRESS
698
678

FIG. 35A

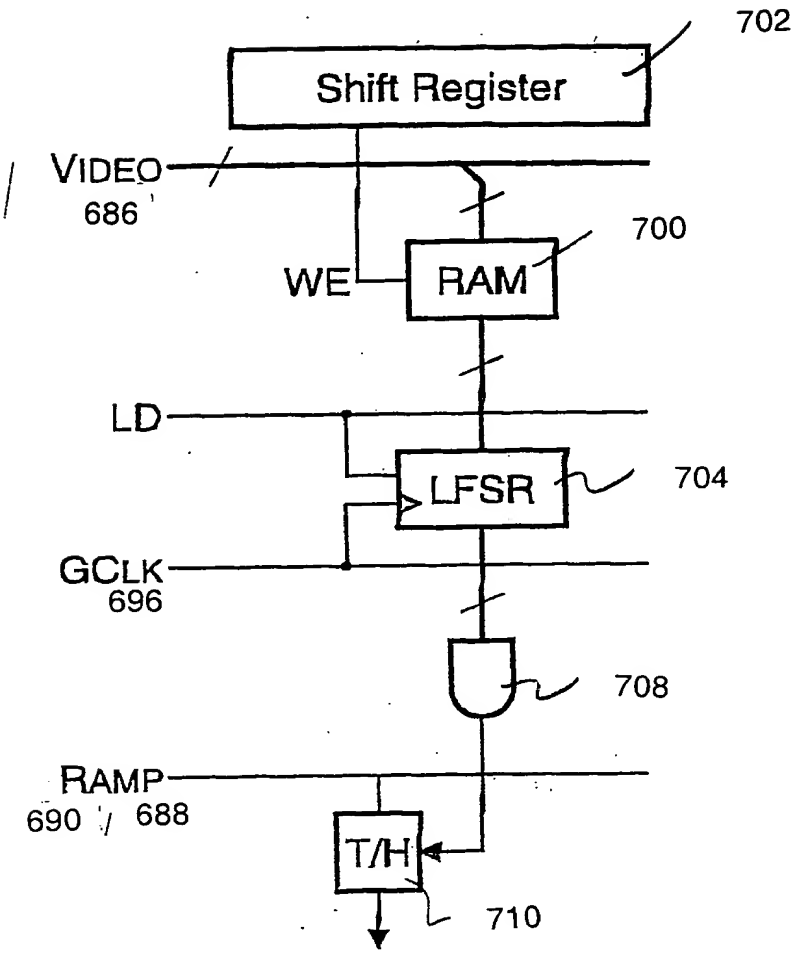

702
Shift Register
VIDEO
686
700
WE
RAM
LD
LFSR
704
GCLK
696
708
RAMP
690
688
T/H
710

FIG. 35B

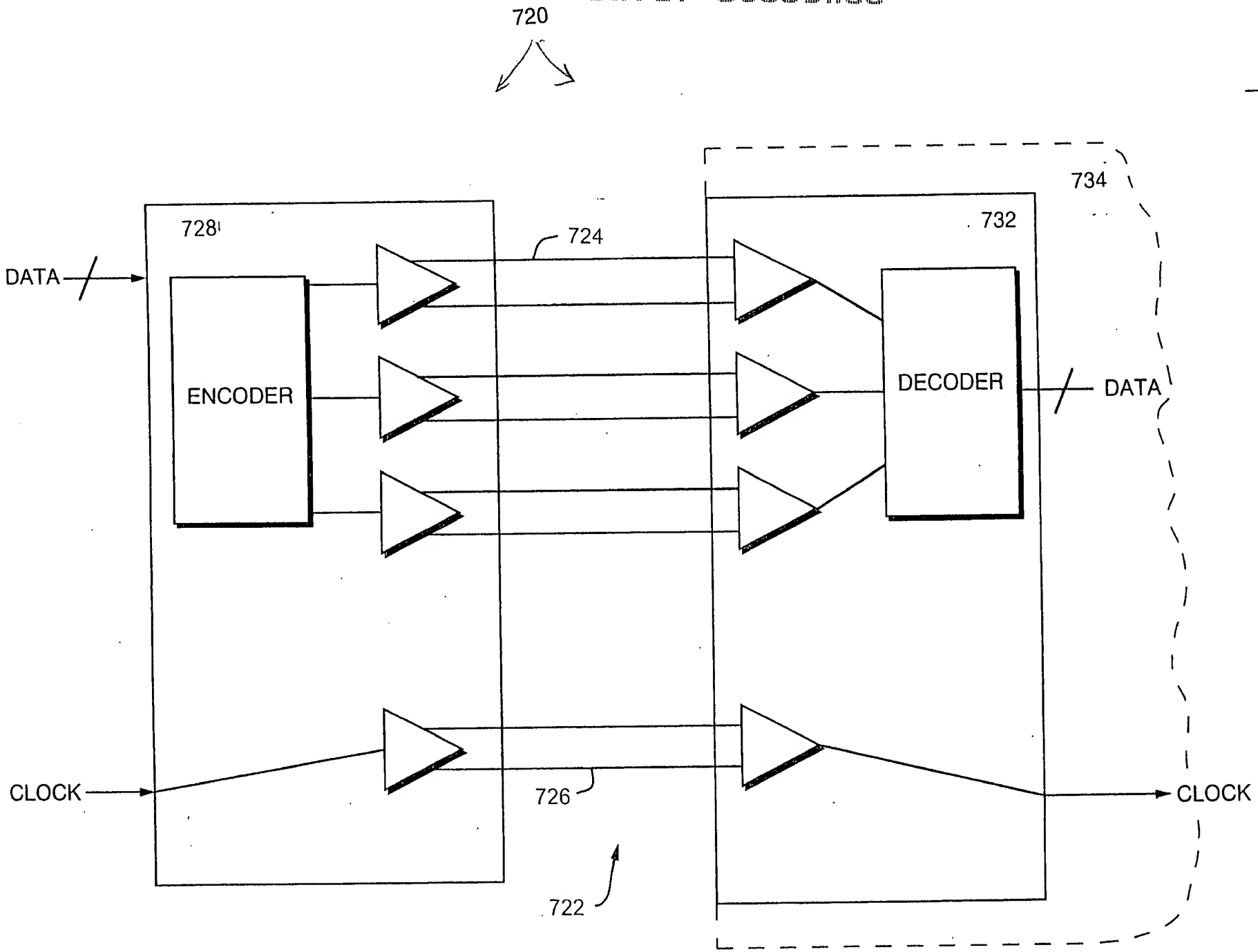


FIG. 36

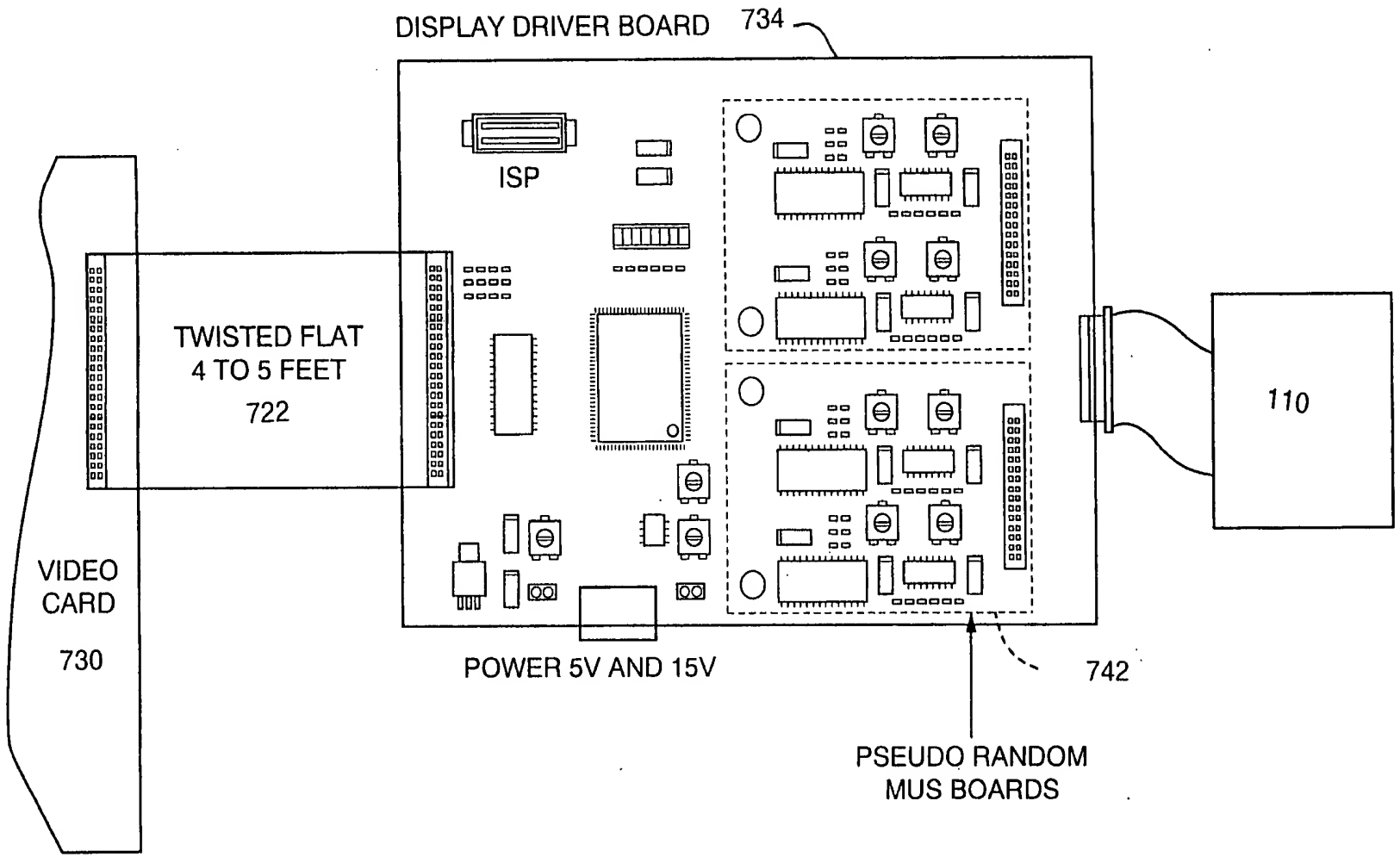


FIG. 37A

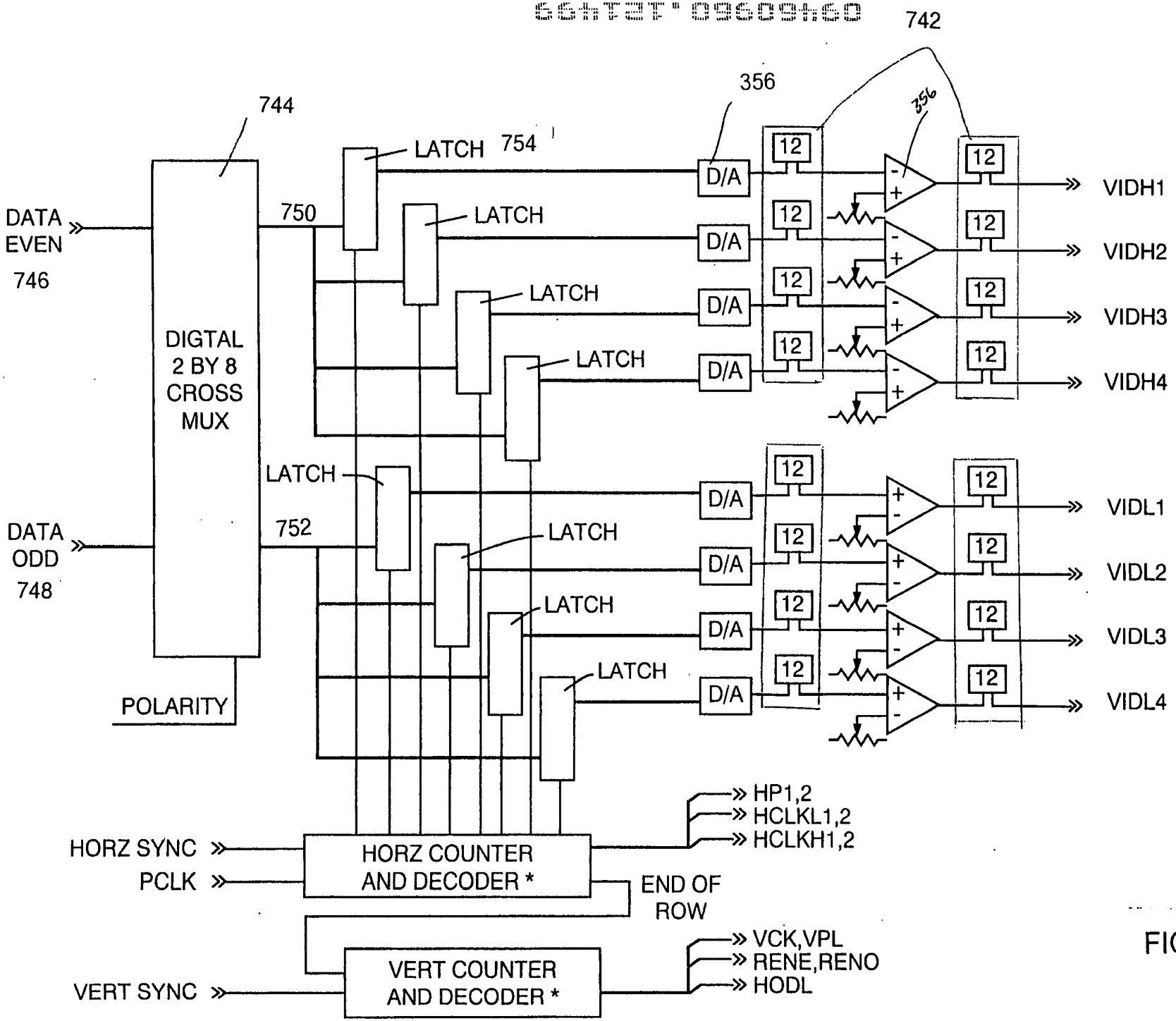


FIG 37B

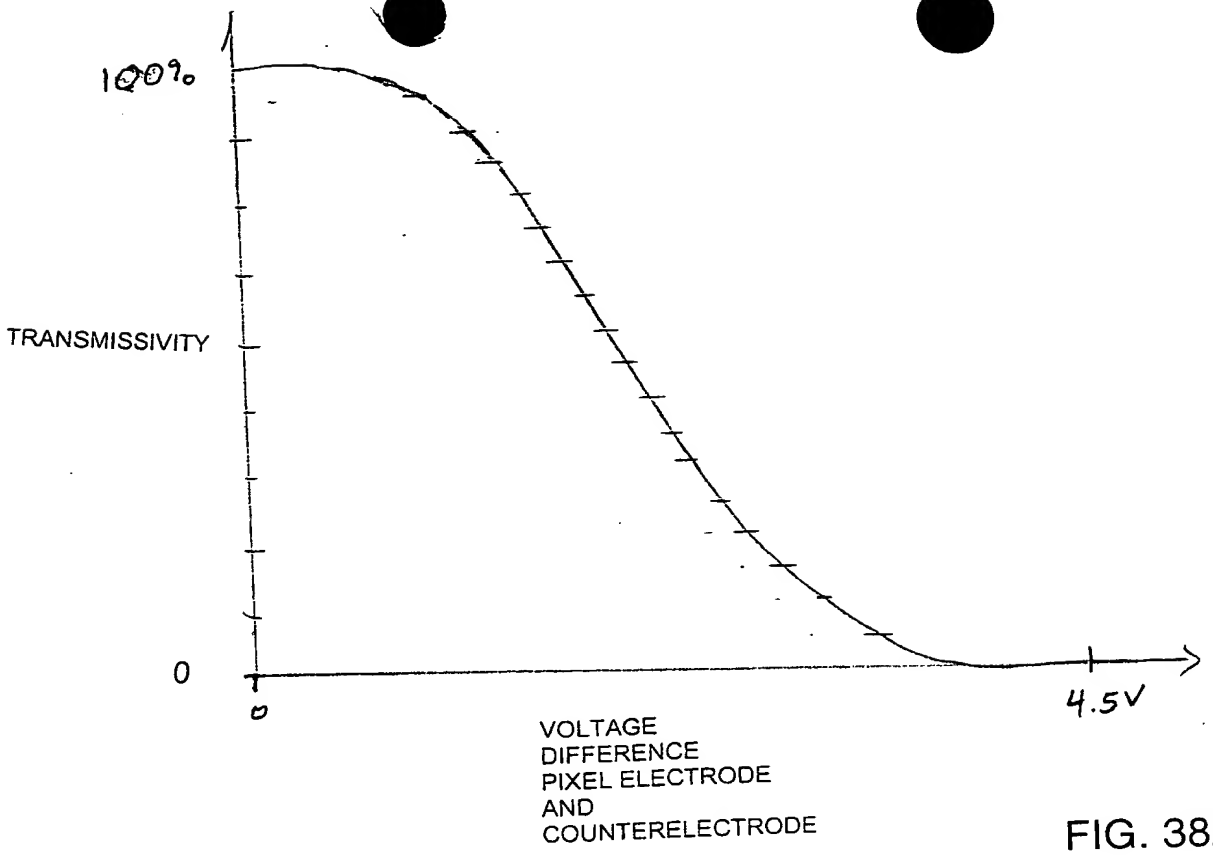


FIG. 38A

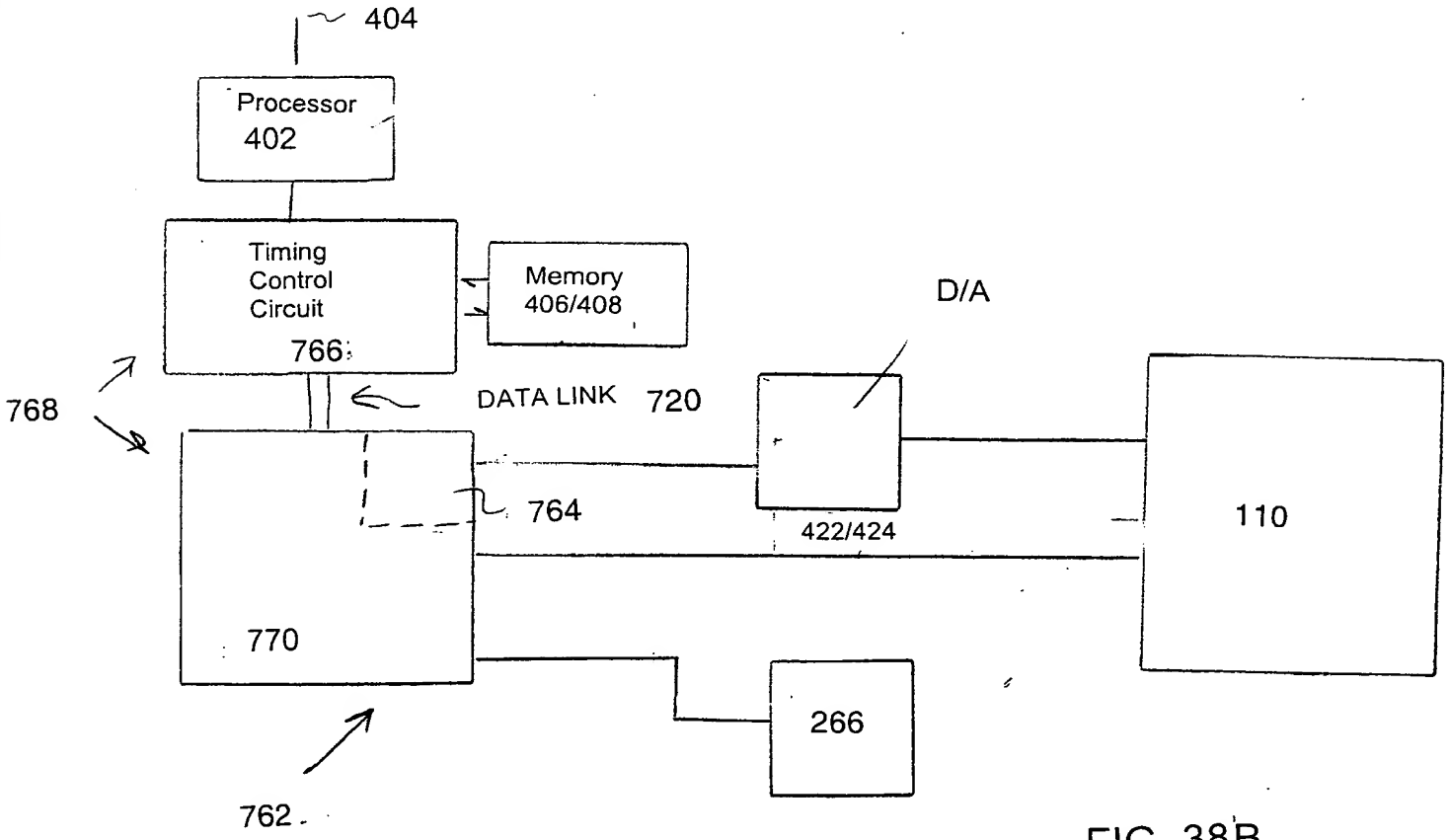
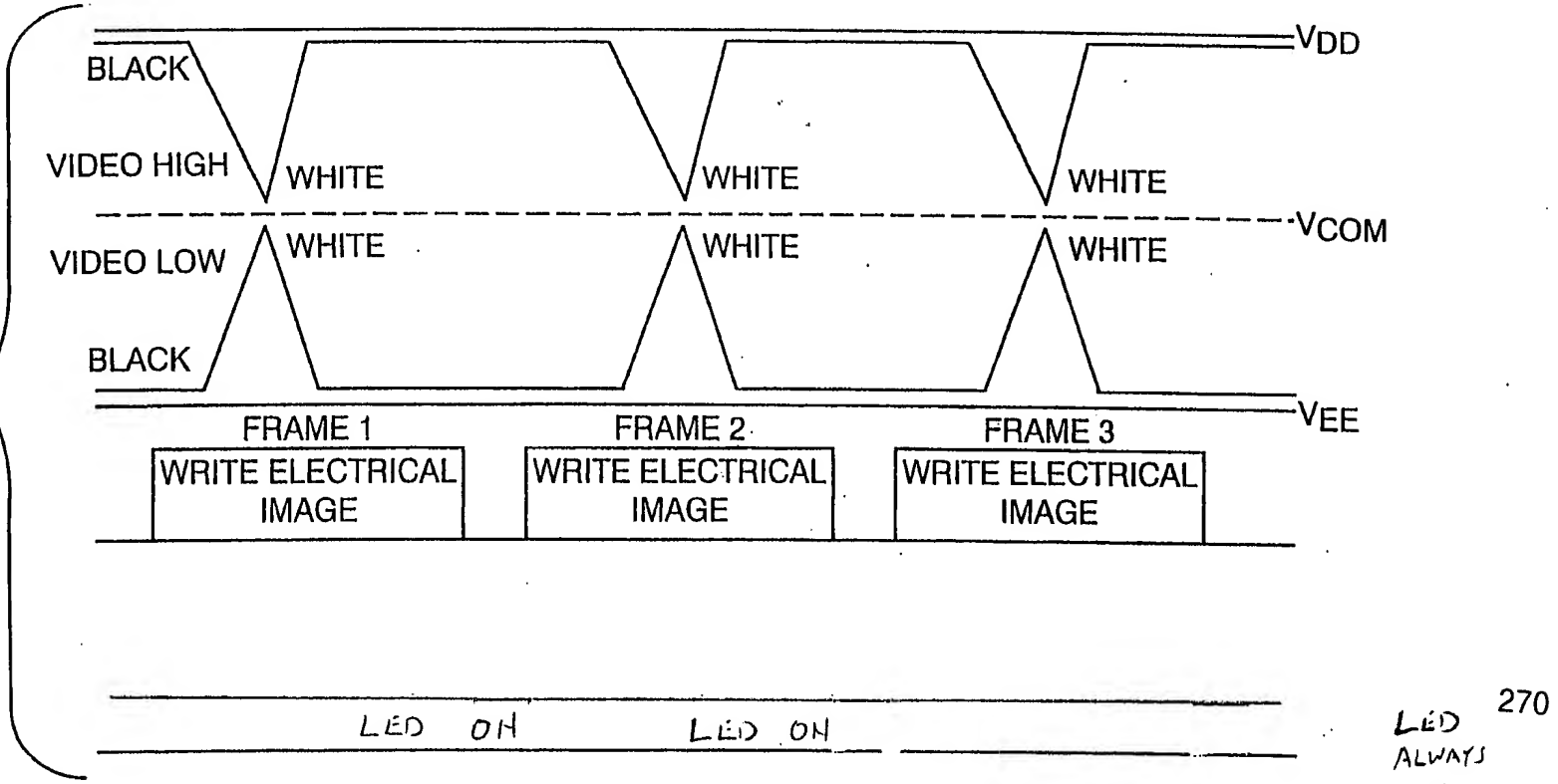


FIG. 38B

FIG. 39A



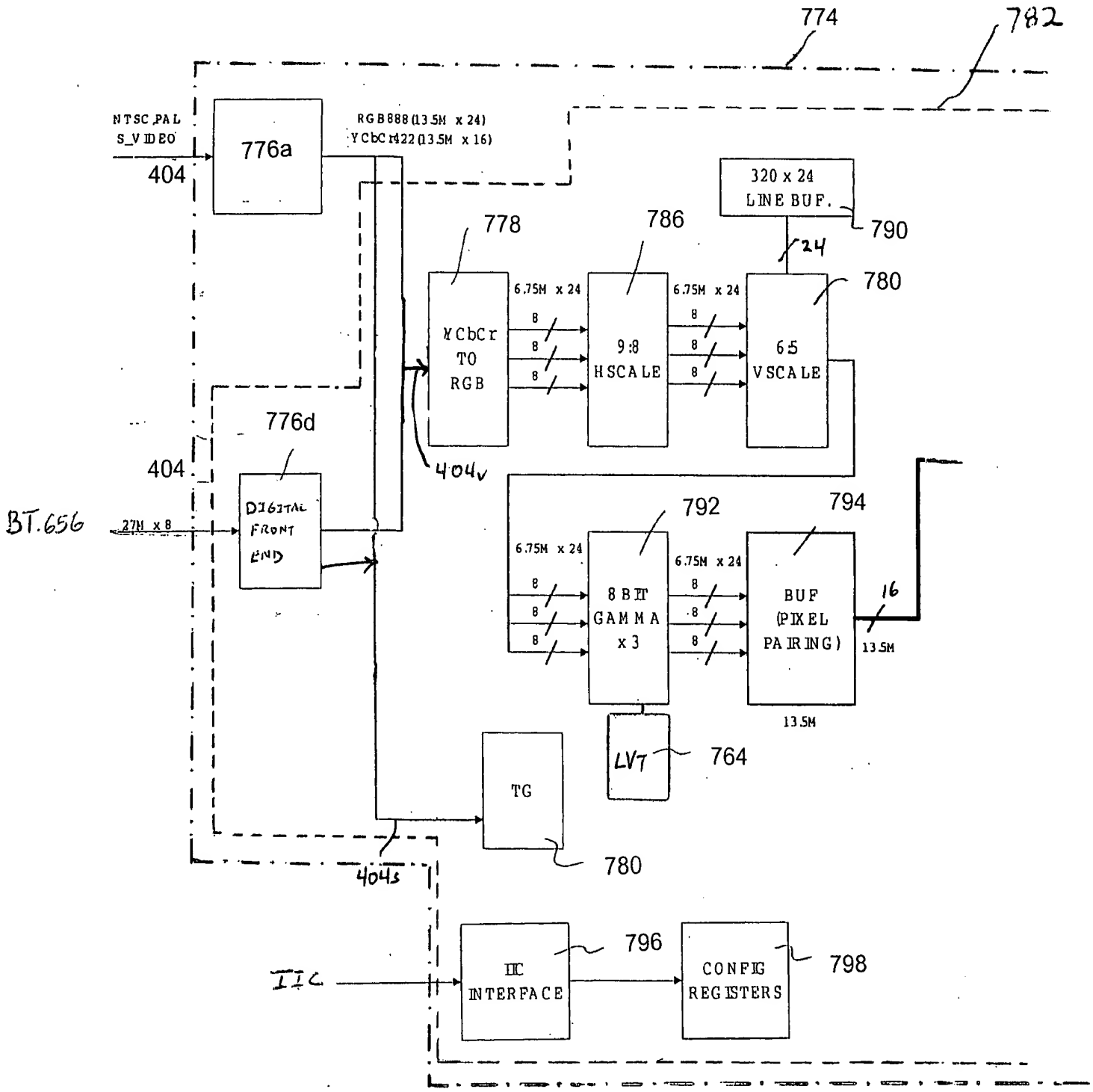


FIG. 39B1

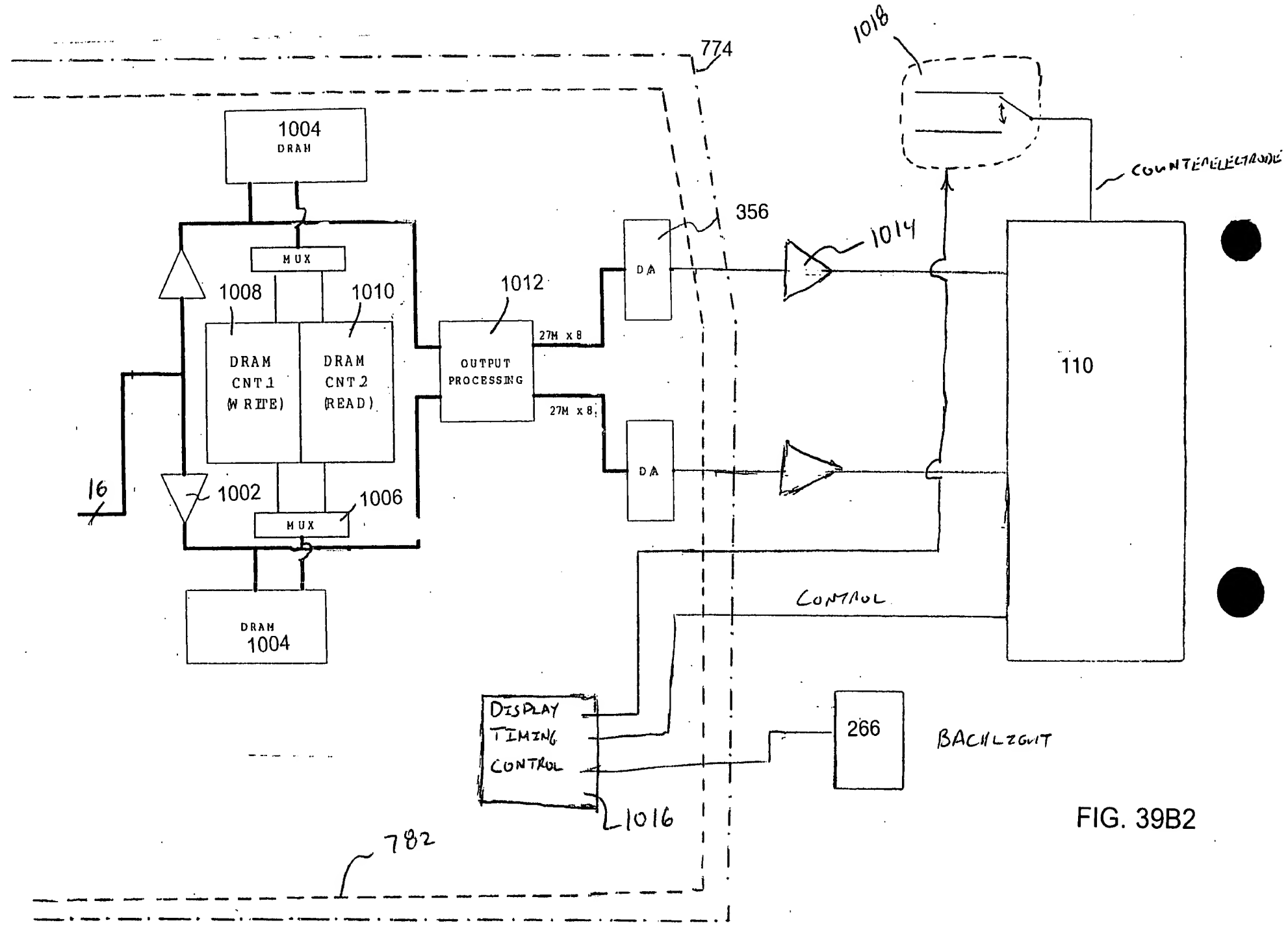


FIG. 39B2

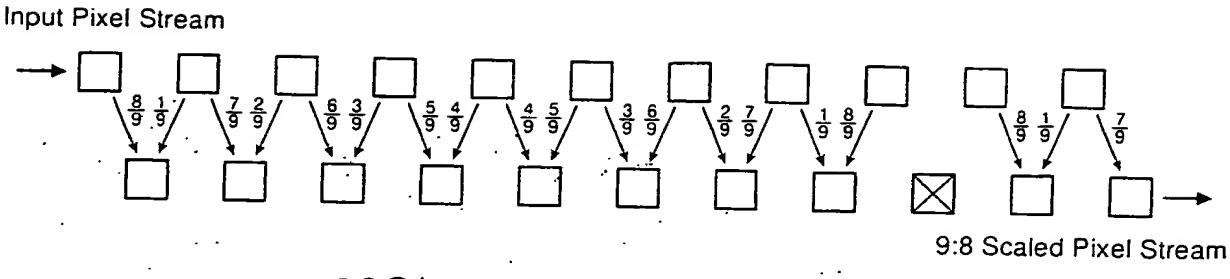


FIG. 39C 9:8 Horizontal Scaling by Interpolation

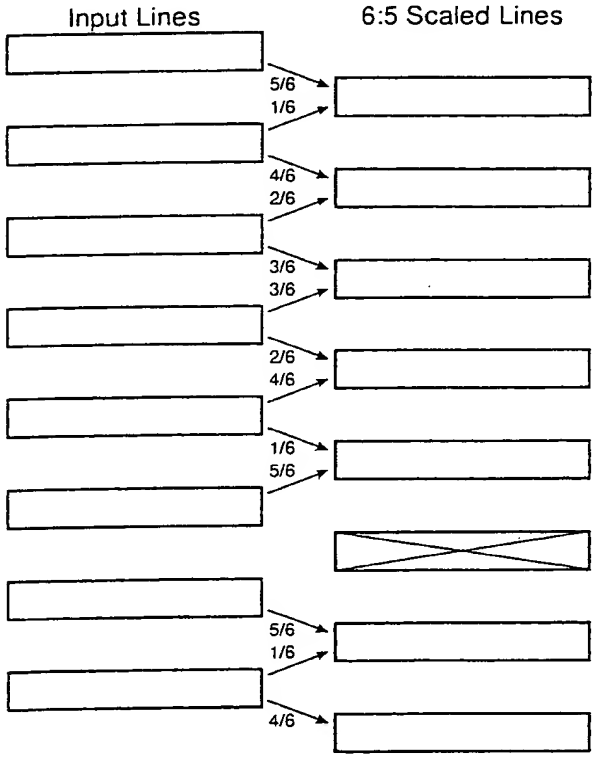


FIG. 39D 6:5 Vertical Scaling by Interpolation

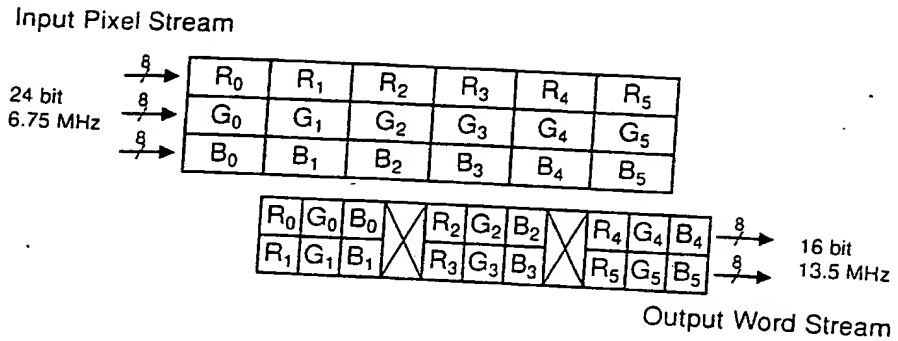


FIG. 39E Pixel Pairing

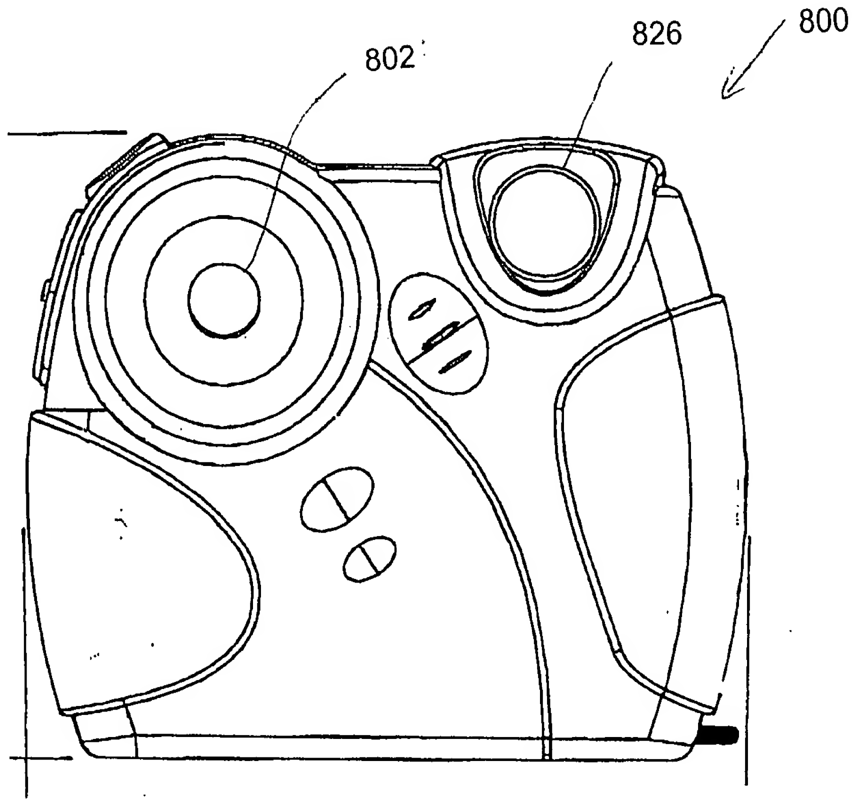


FIG. 40A

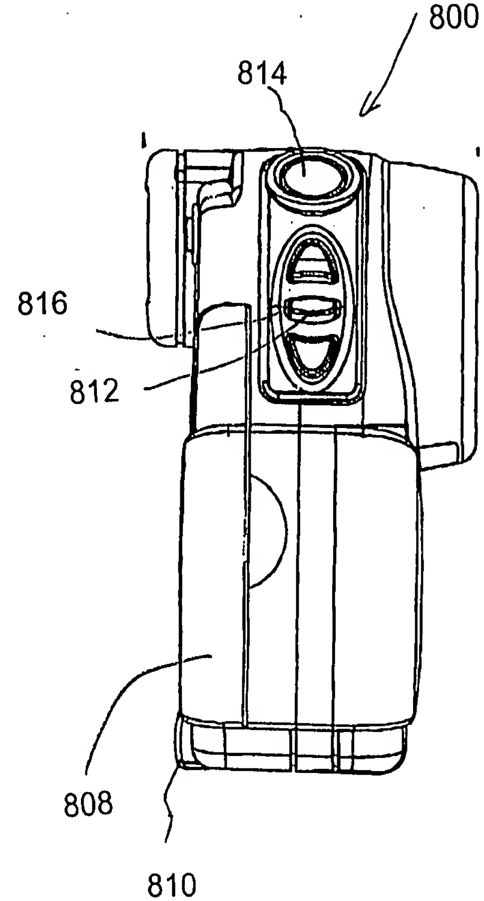


FIG. 40C

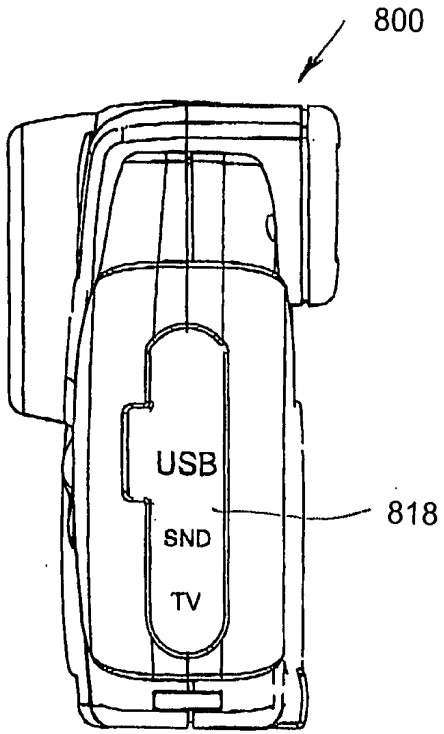


FIG. 40D

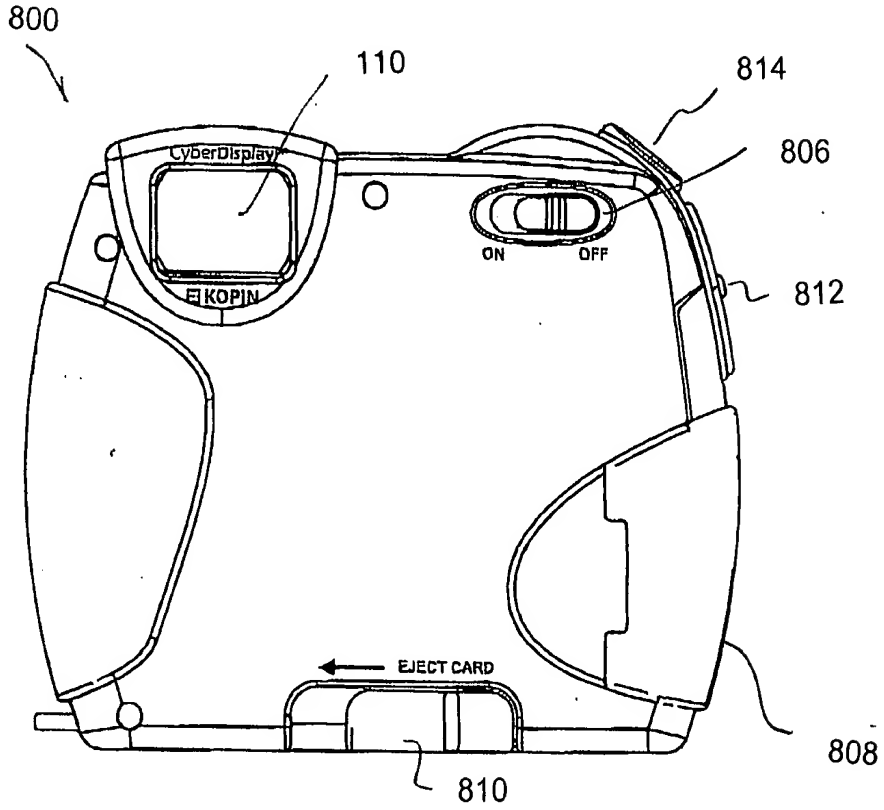


FIG. 40B

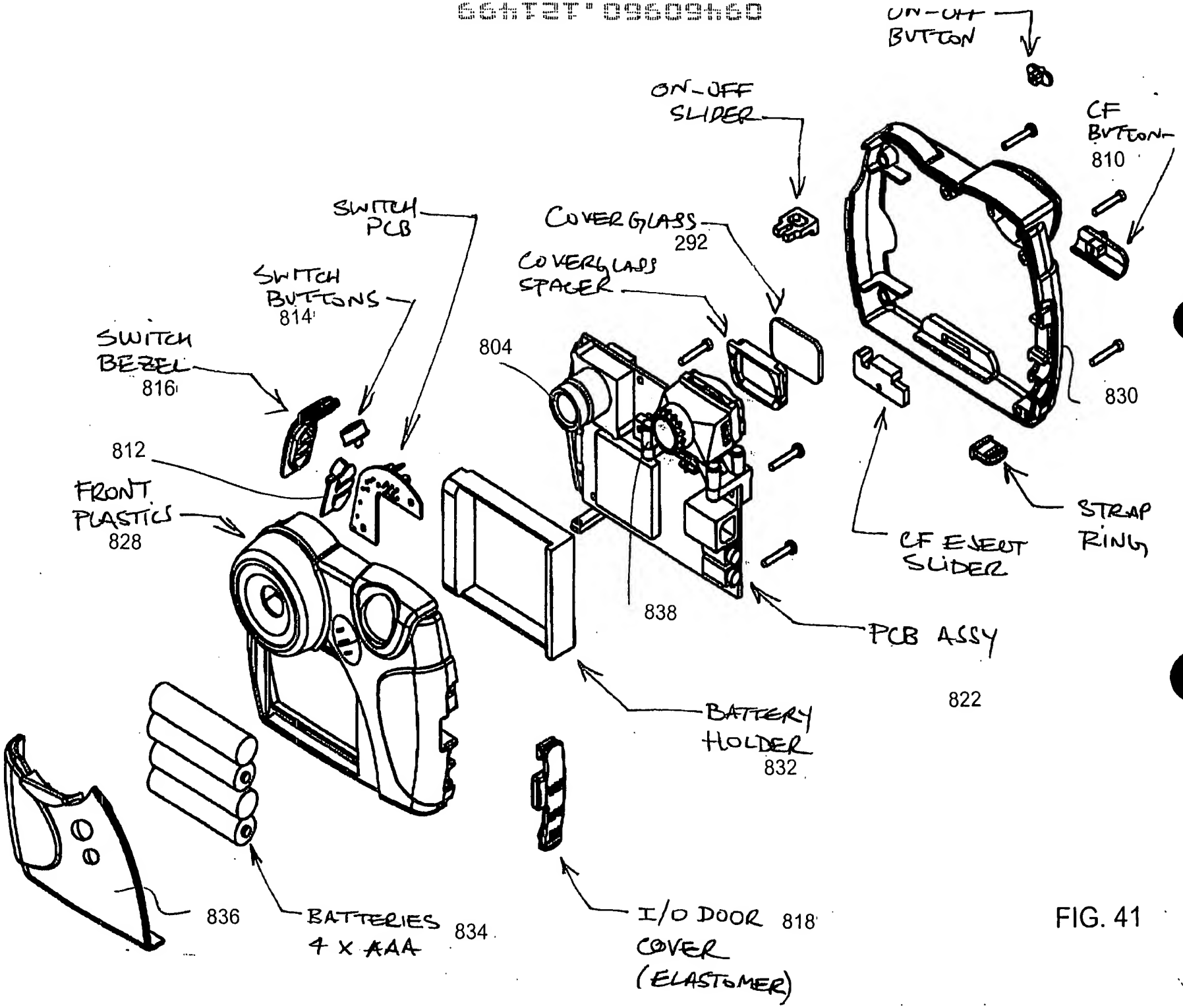


FIG. 41

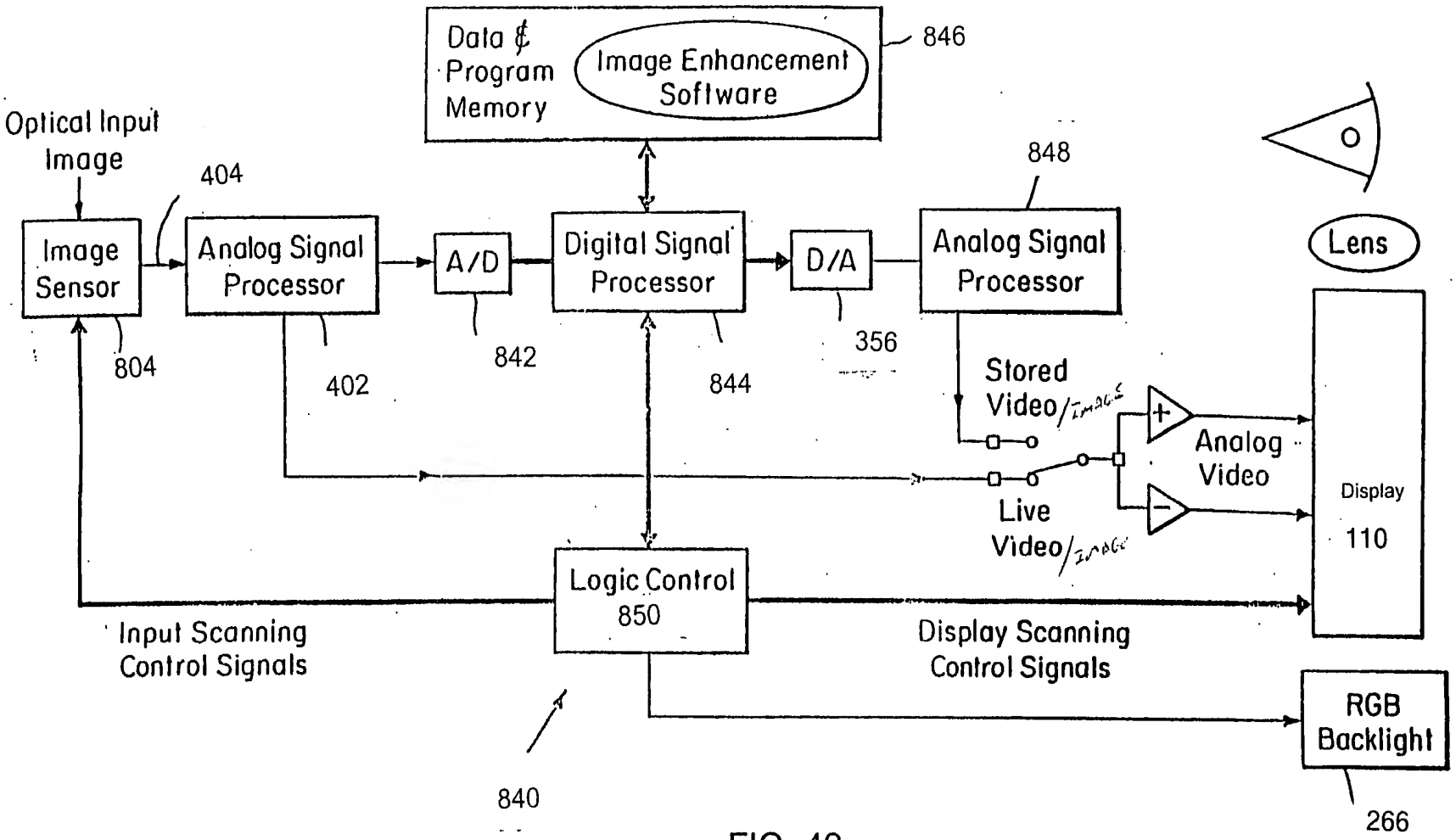

Data & Program Memory
Image Enhancement Software
846
Optical Input Image
404
Image Sensor
804
Analog Signal Processor
402
A/D
842
Digital Signal Processor
844
D/A
356
848
Analog Signal Processor
Lens
Stored Video/Image
Live Video/Image
Analog Video
Display
110
Logic Control
850
Input Scanning Control Signals
Display Scanning Control Signals
RGB Backlight
266
840

FIG. 42

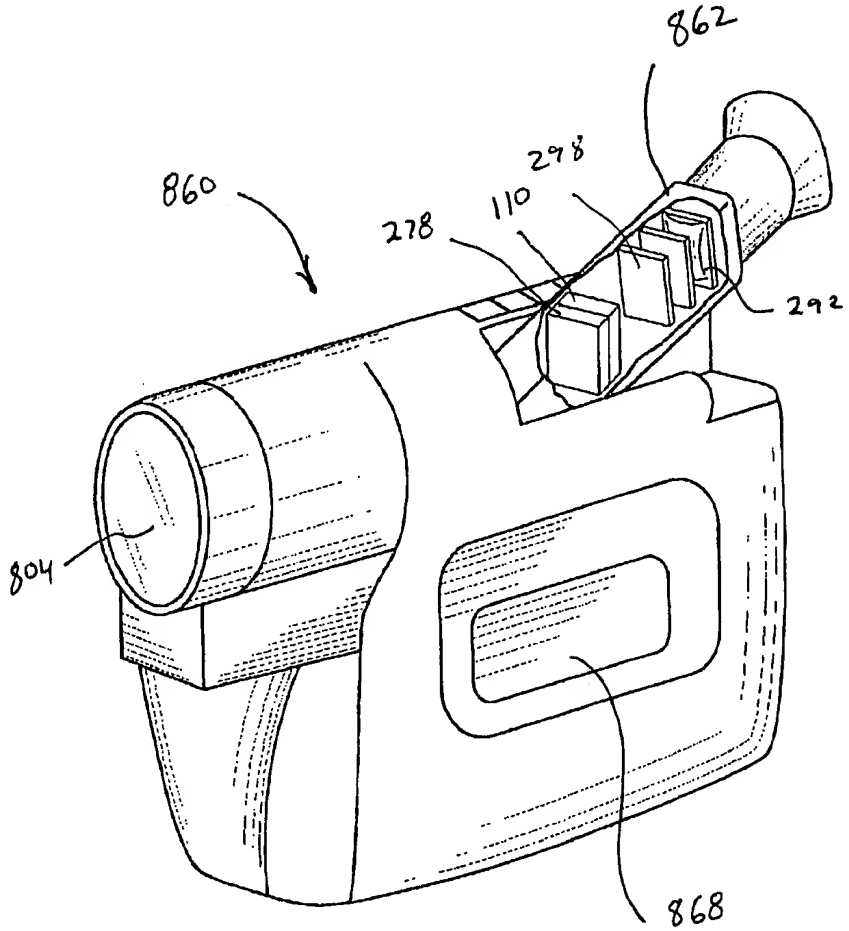
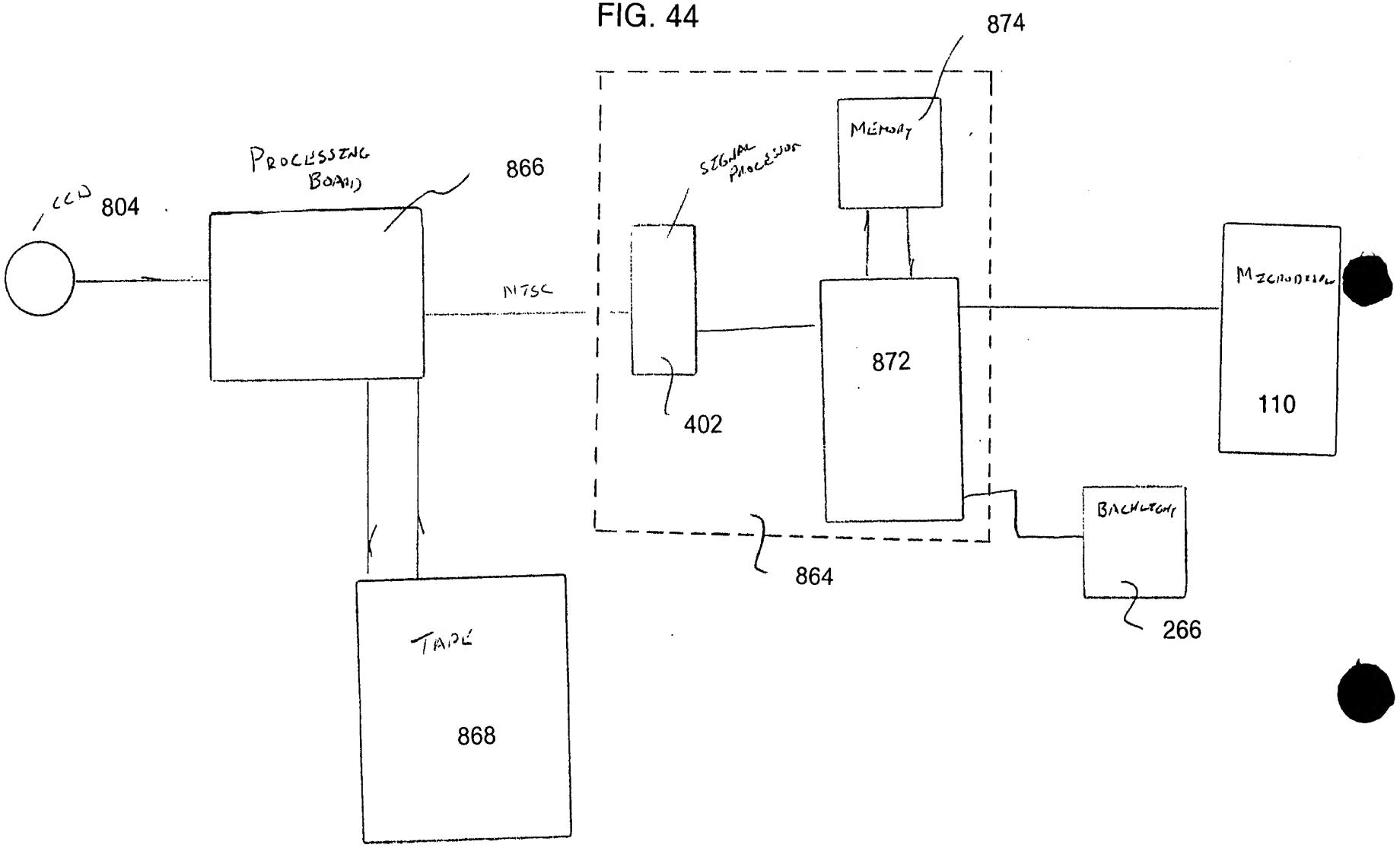


FIG. 43

FIG. 44


874
MEMORY
PROCESSING BOARD
866
SIGNAL PROCESSOR
CCD
804
NTSC
872
MICROPHONE
110
402
BACKLIGHT
864
266
TAPE
868

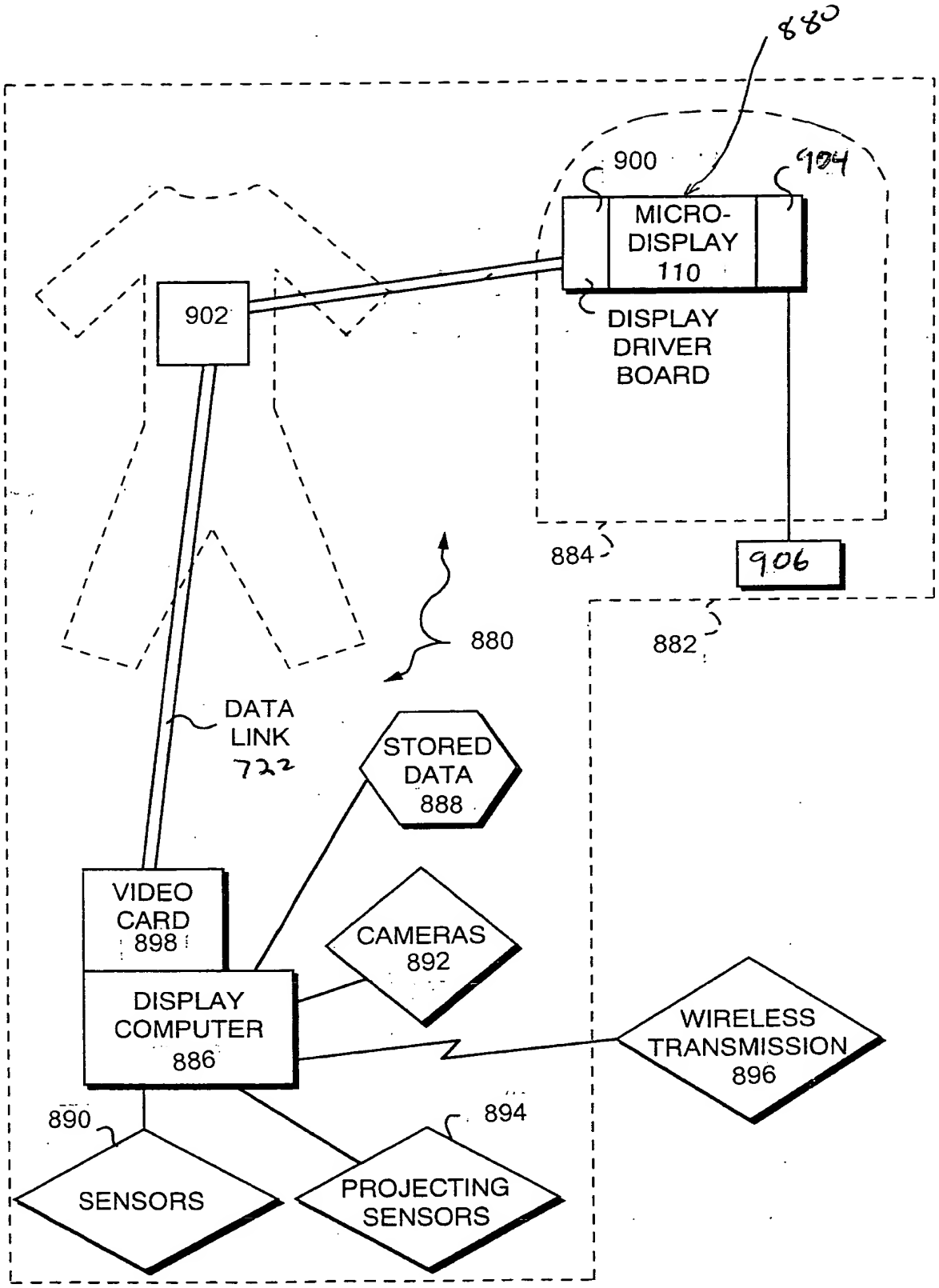

880
900
904
MICRO-DISPLAY 110
902
DISPLAY DRIVER BOARD
884
906
882
880
DATA LINK 722
STORED DATA 888
VIDEO CARD 898
CAMERAS 892
DISPLAY COMPUTER 886
WIRELESS TRANSMISSION 896
890
894
SENSORS
PROJECTING SENSORS

FIG. 45

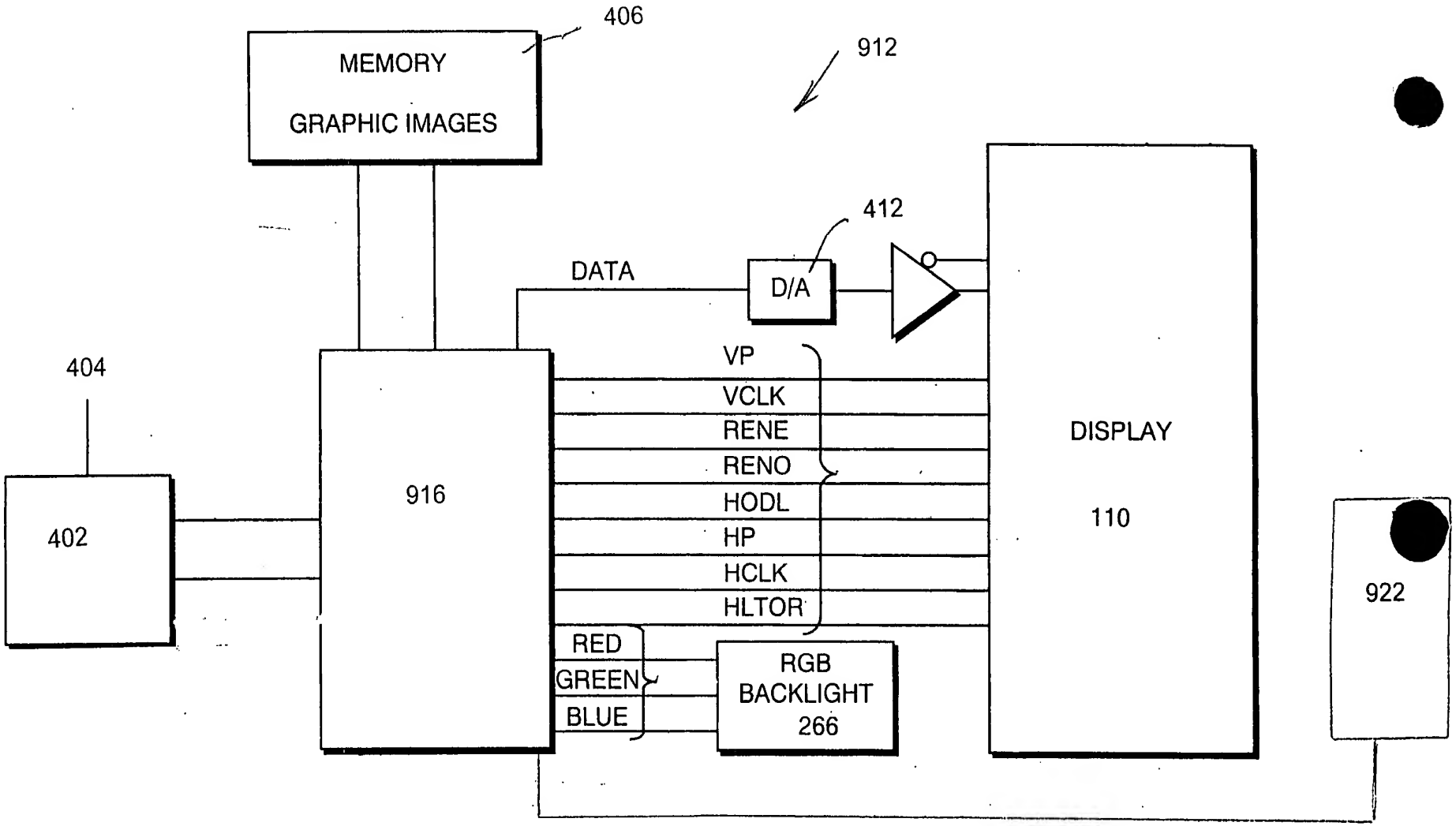


FIG. 46

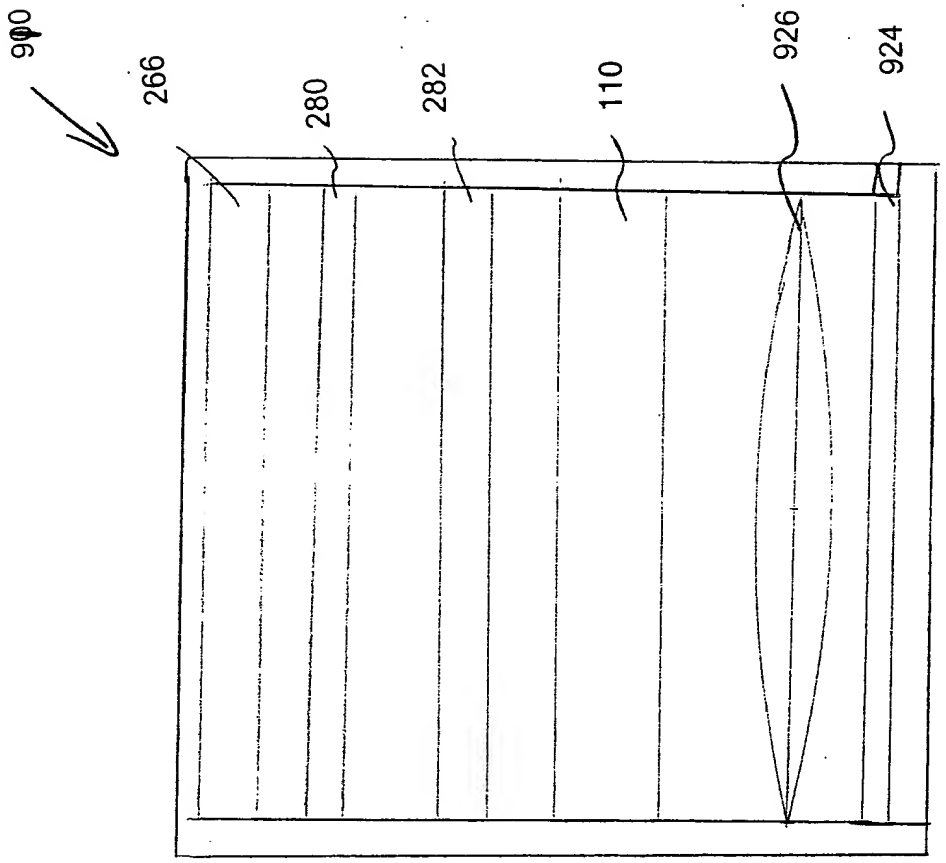


FIG. 47

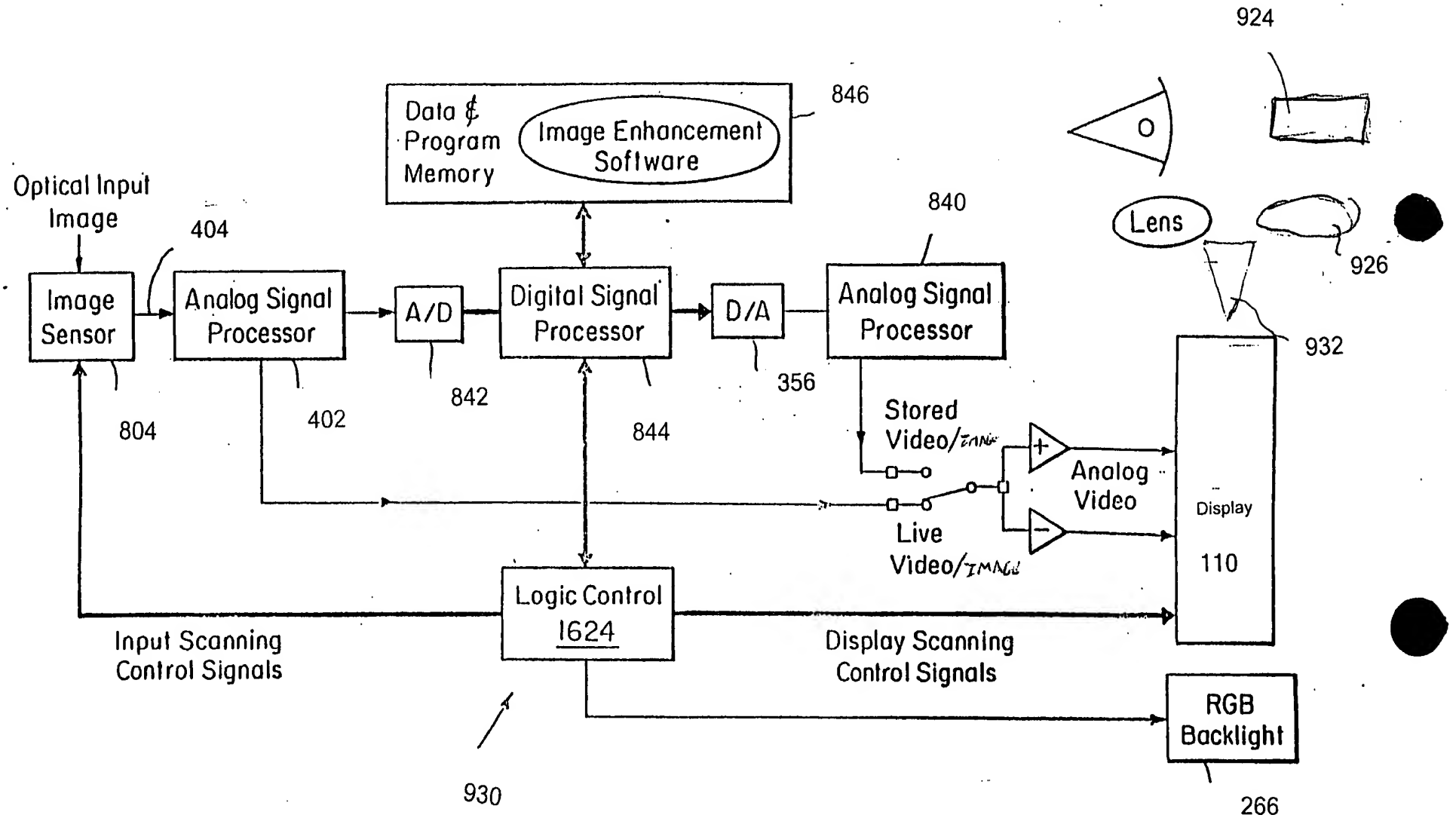


FIG. 48

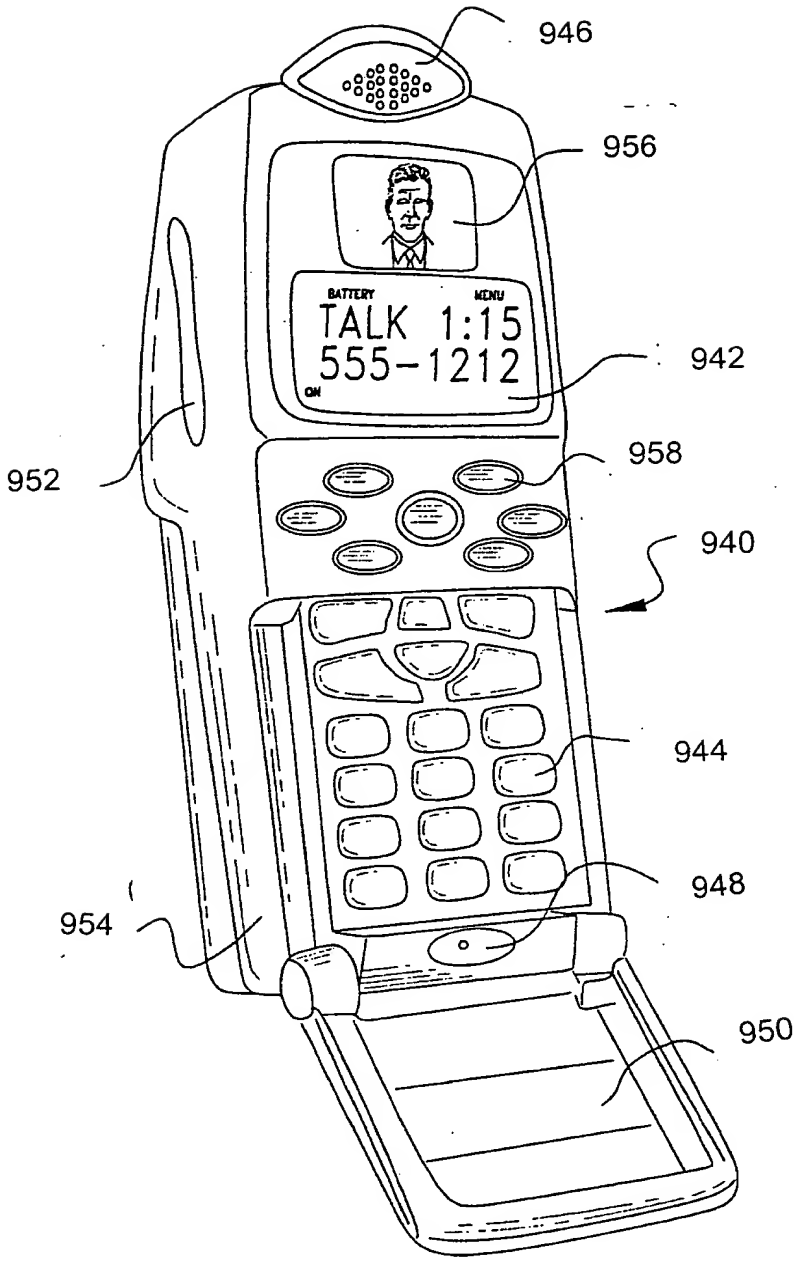

946
956
BATTERY
MENU
TALK 1:15
555-1212
ON
942
952
958
940
944
948
954
950

FIG. 49A

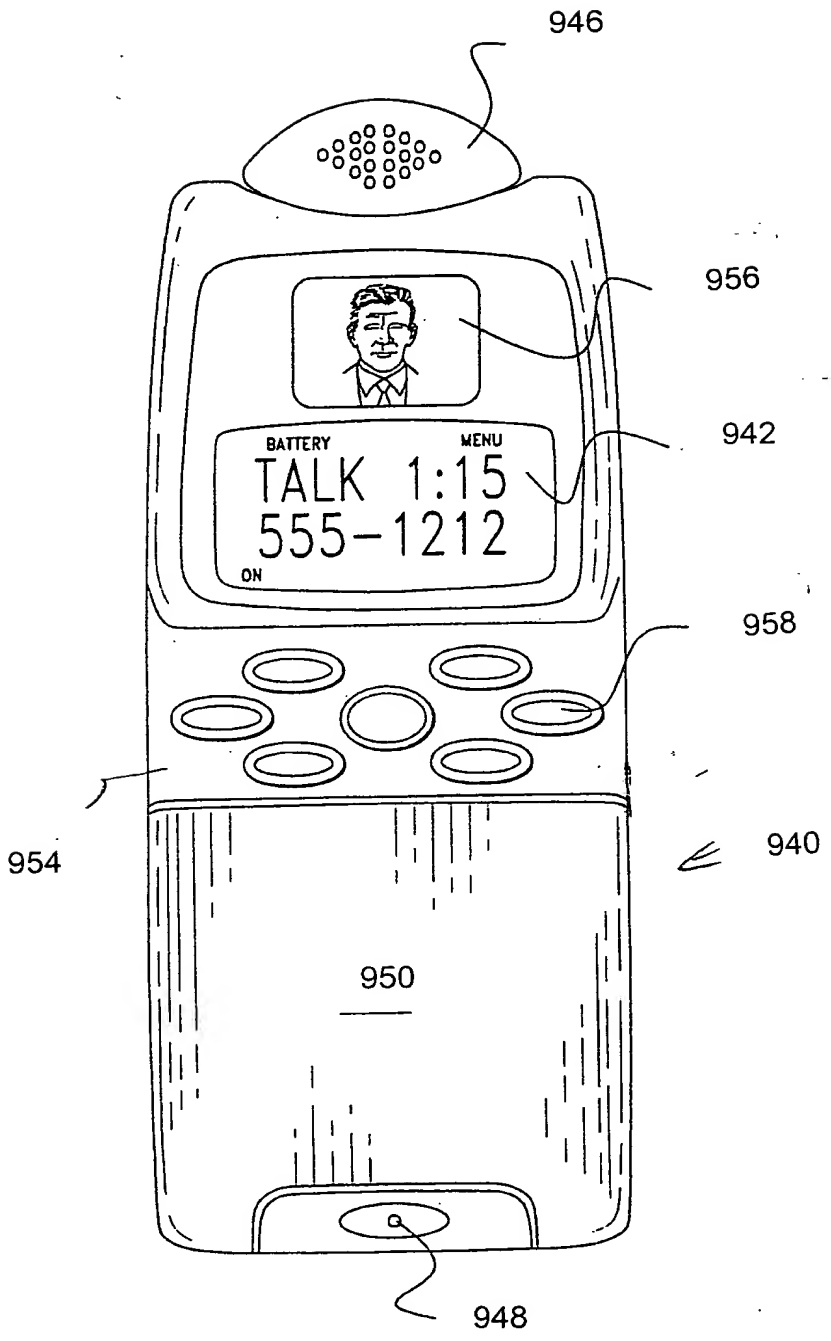

946
956
942
BATTERY
MENU
TALK 1:15
555-1212
ON
958
954
940
950
948

FIG. 49B

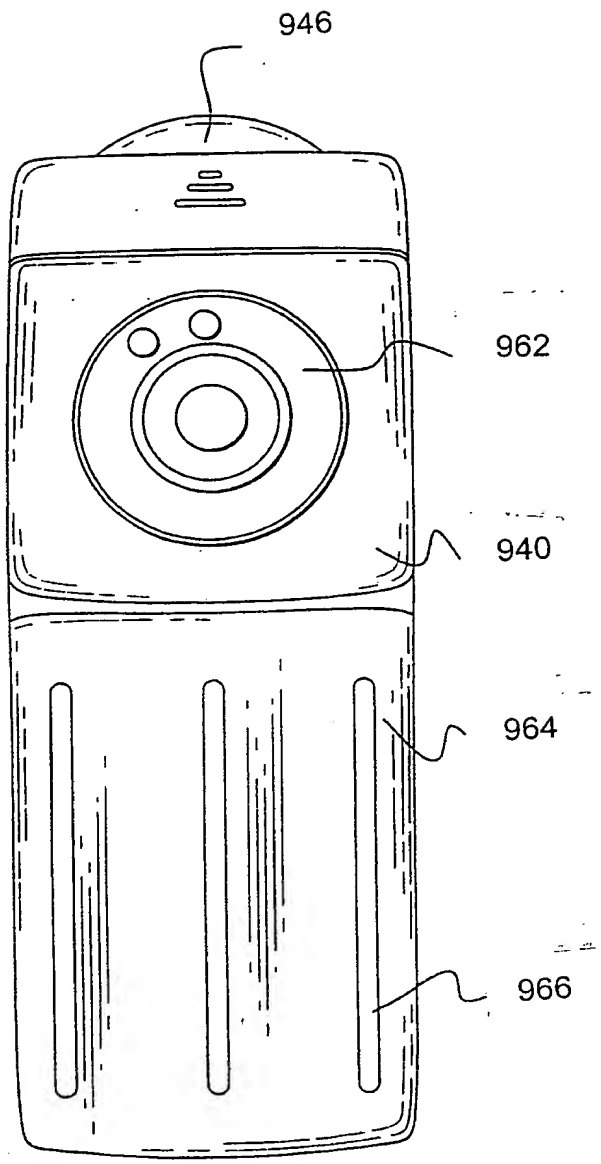


FIG. 49C

09609560.121499

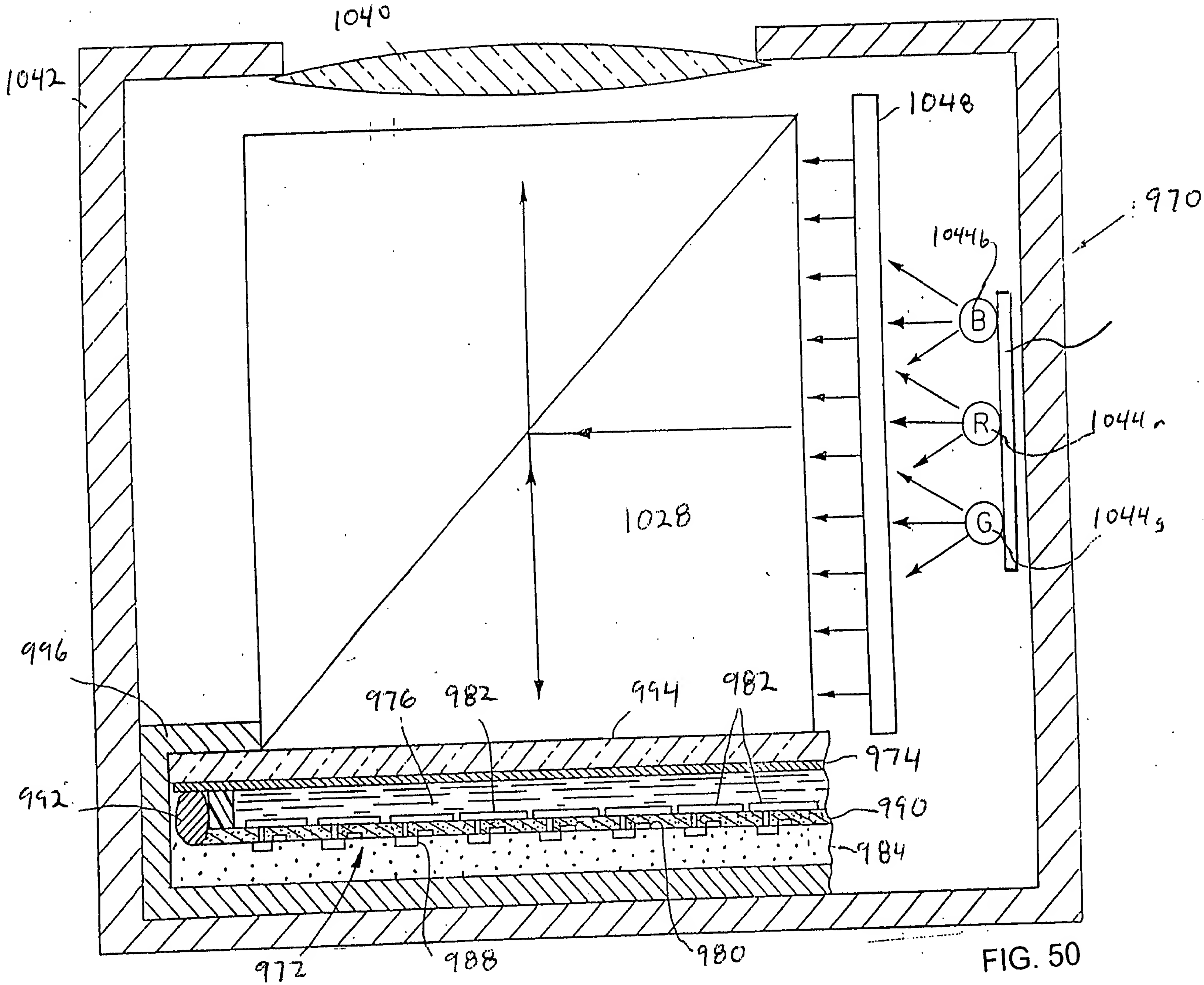


FIG. 50

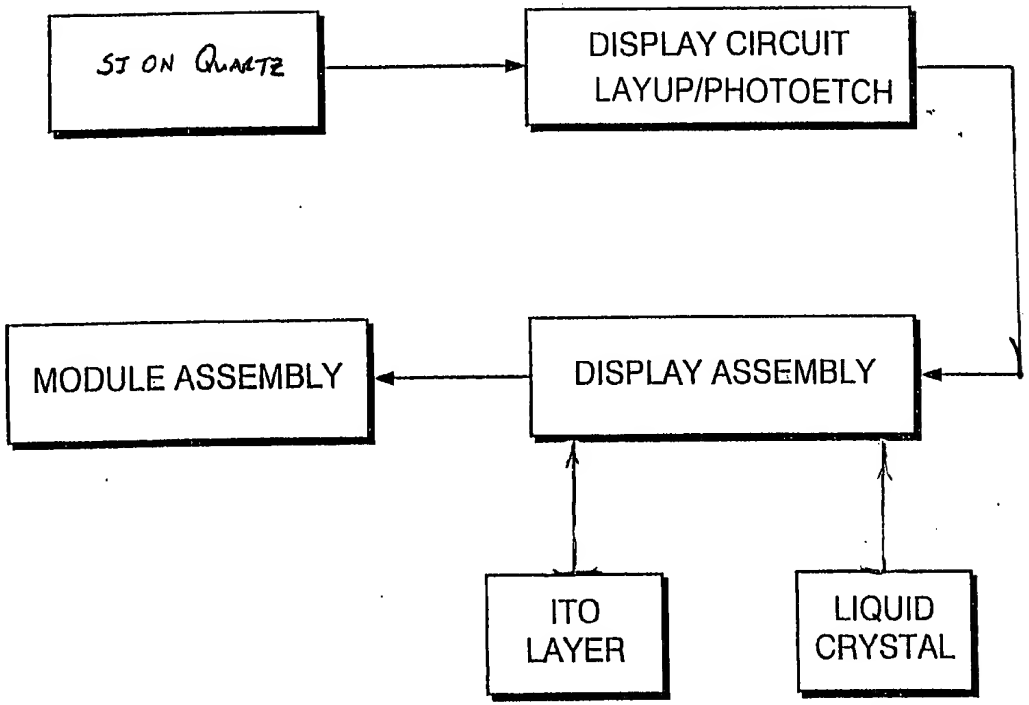


FIG. 5'